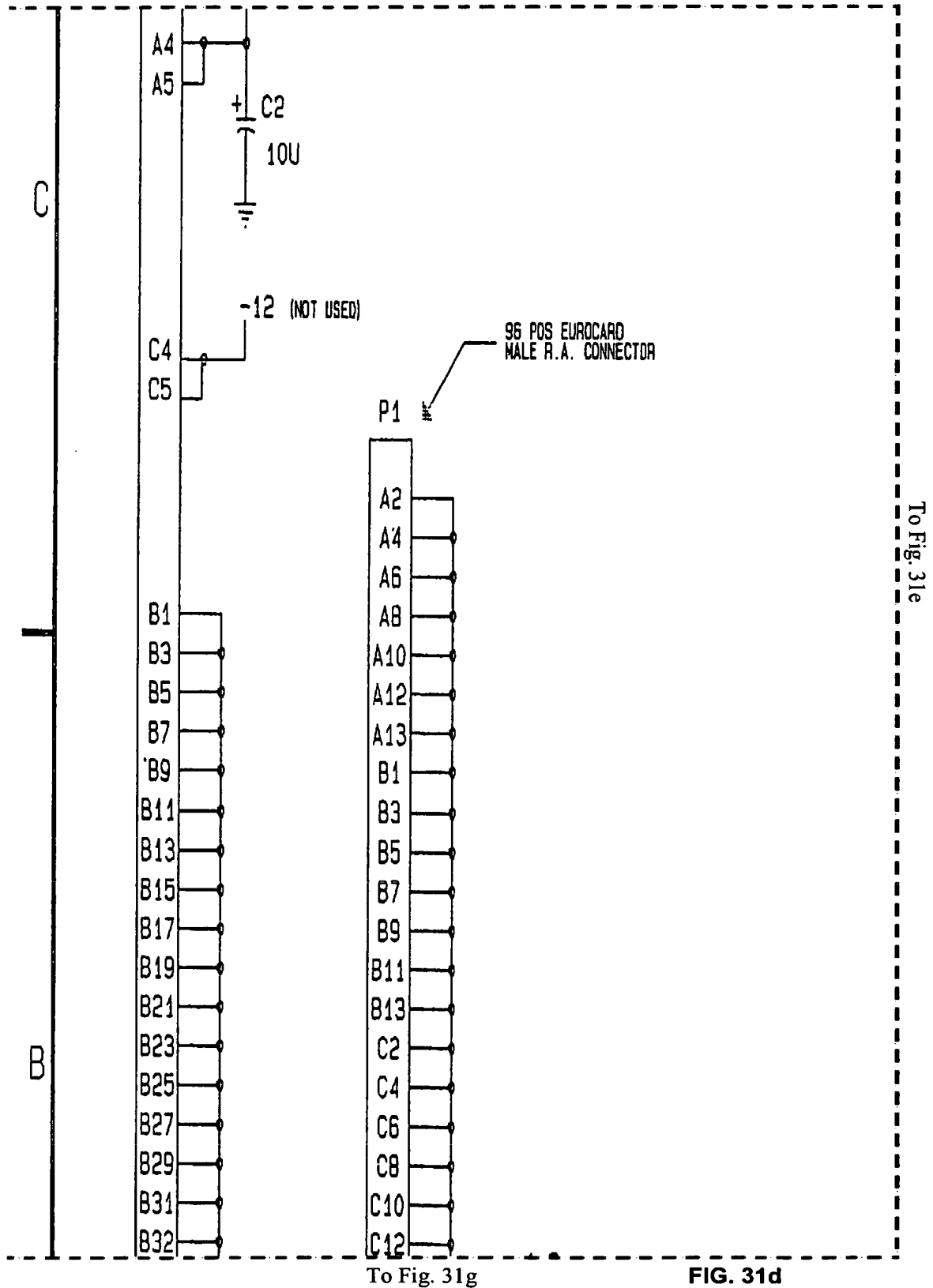


To Fig. 31a



To Fig. 31b

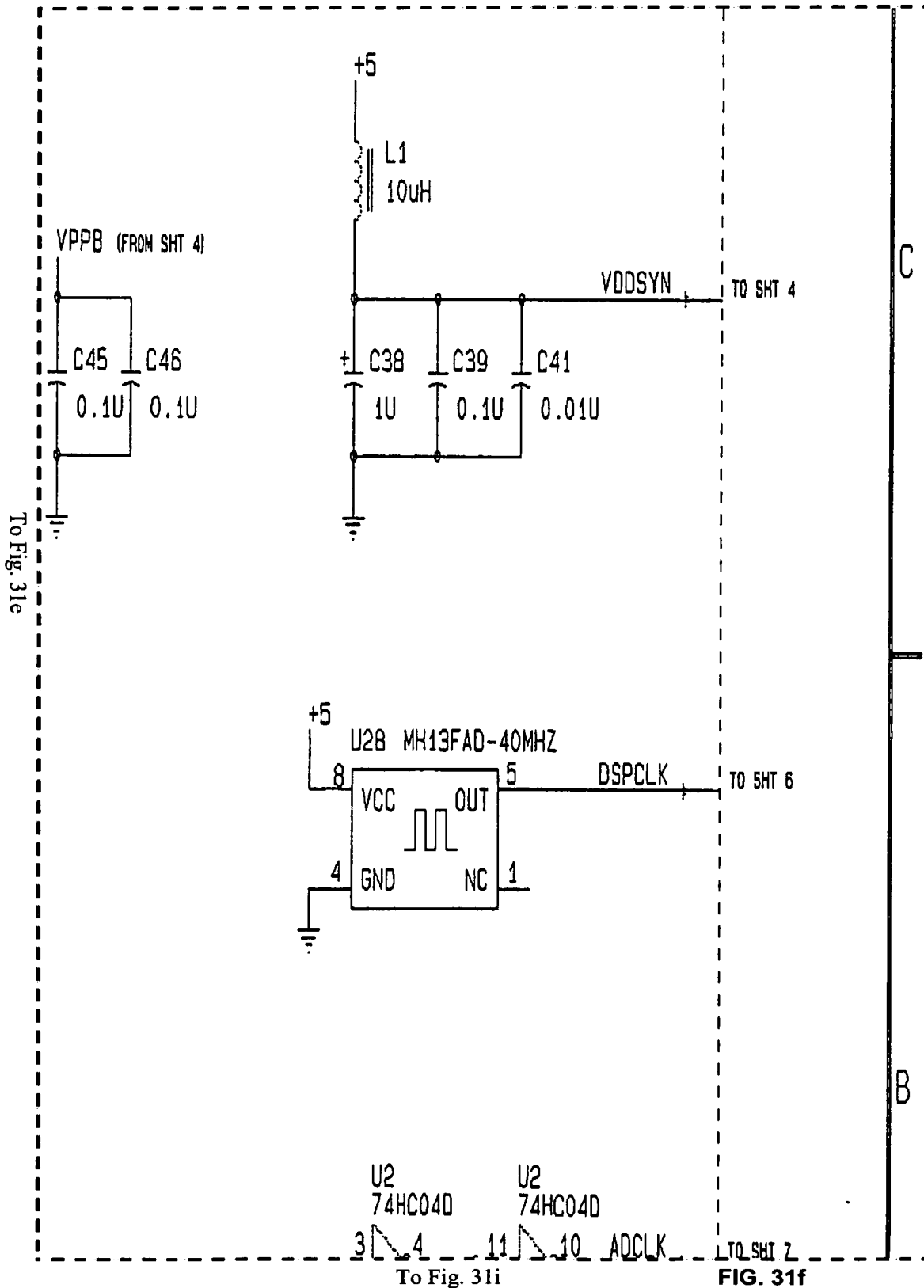
To Fig. 31d

To Fig. 31f

To Fig. 31h

FIG. 31e

To Fig. 31c



To Fig. 31i

FIG. 31f

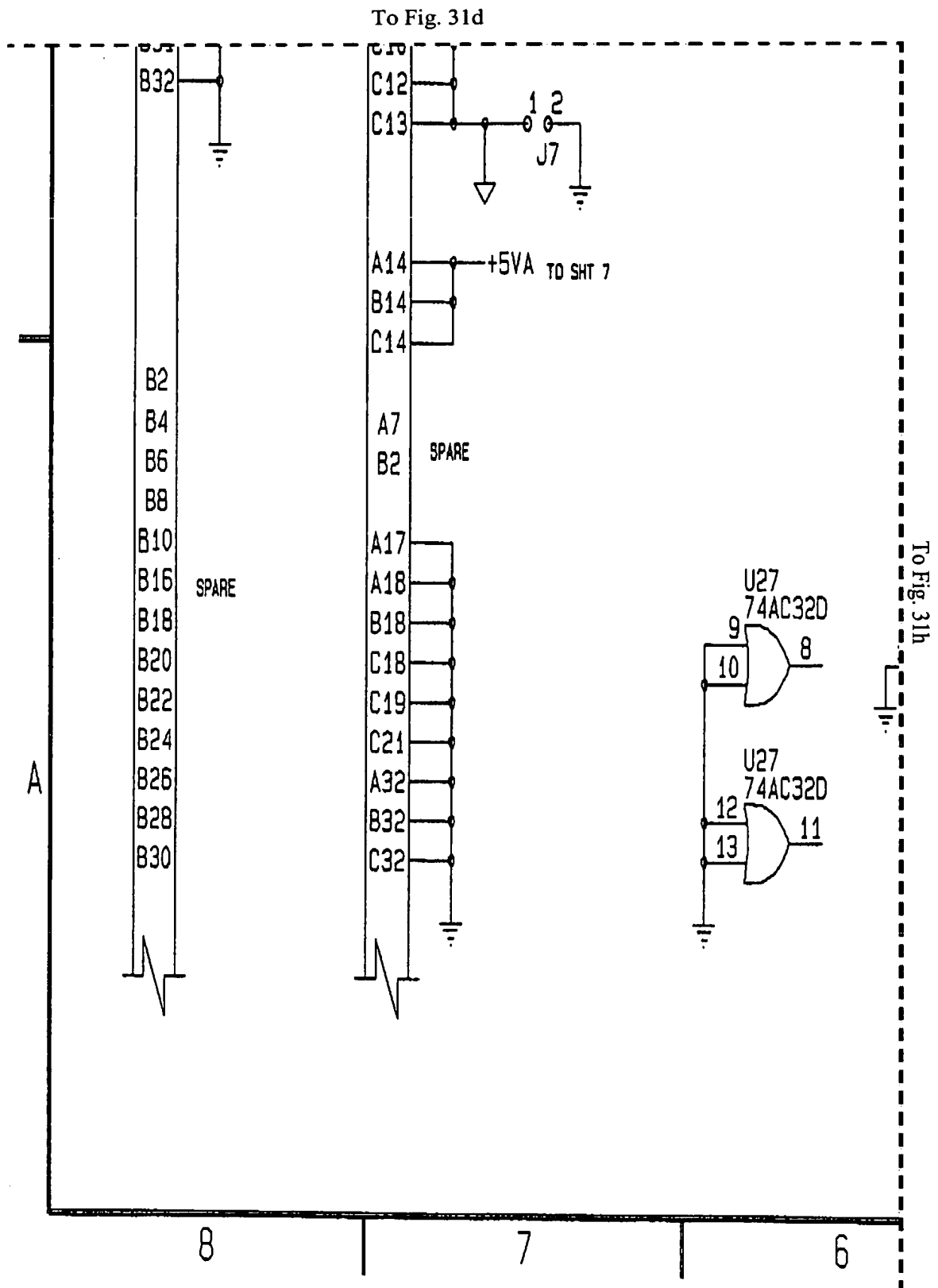
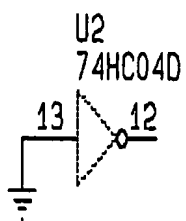


FIG. 31g

To Fig. 31e

To Fig. 31g



To Fig. 31i

This schematic  
proprietary  
configuration  
are issued in  
or use shall  
of CD Power

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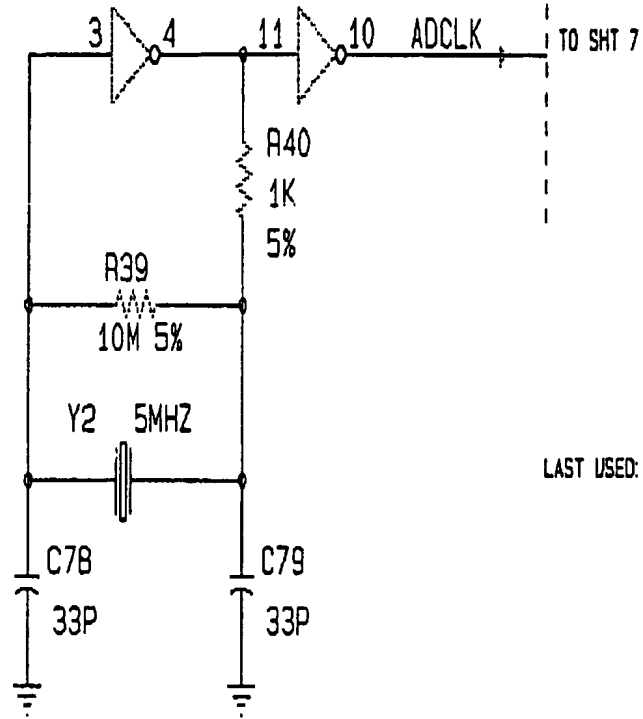
4

FIG. 31h



To Fig. 31f

To Fig. 31h



LAST USED: C83  
R62  
U28  
P3  
J17  
TP11  
DS2



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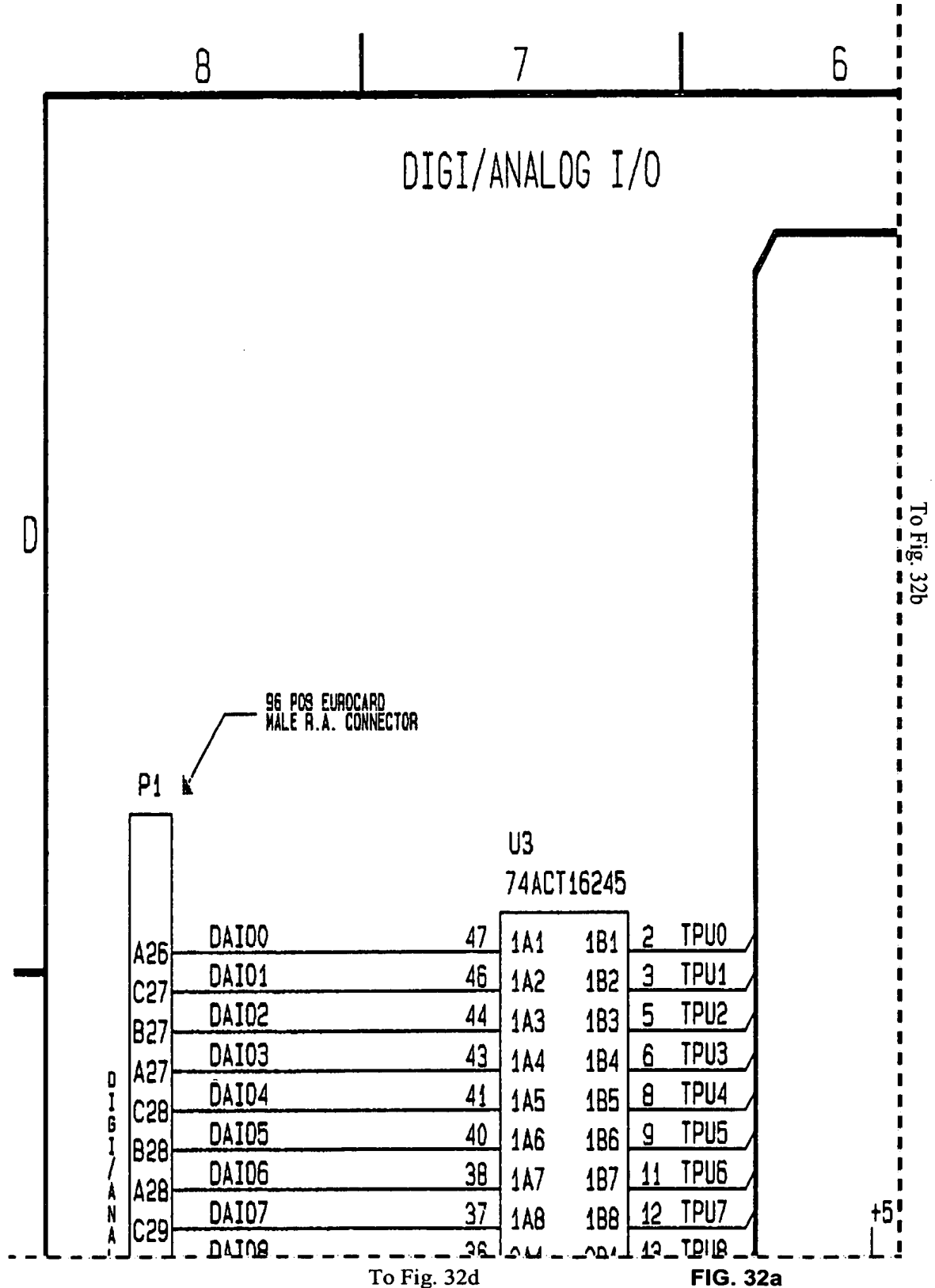
SHEET 1 OF 7

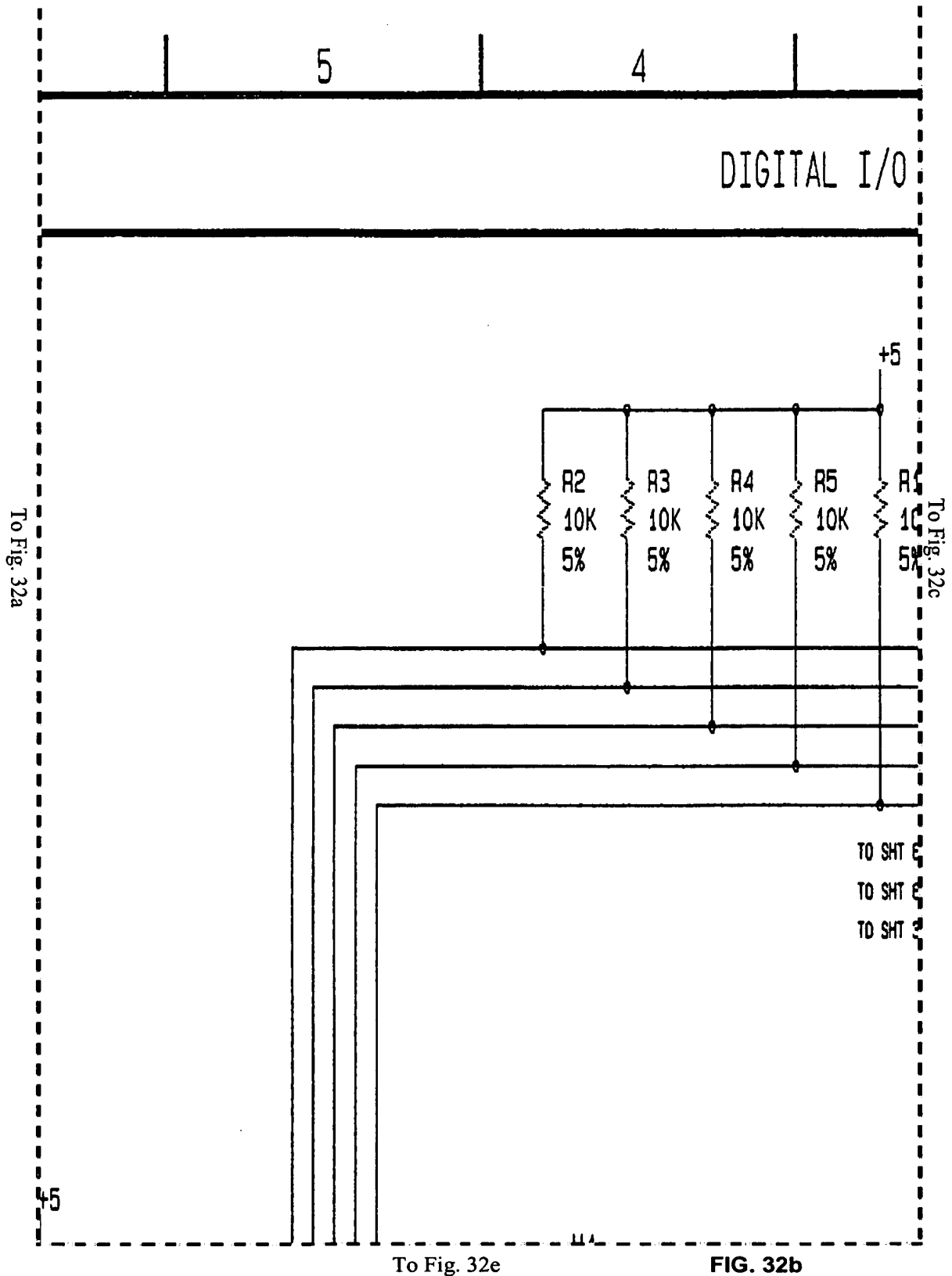
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2

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FIG. 31i





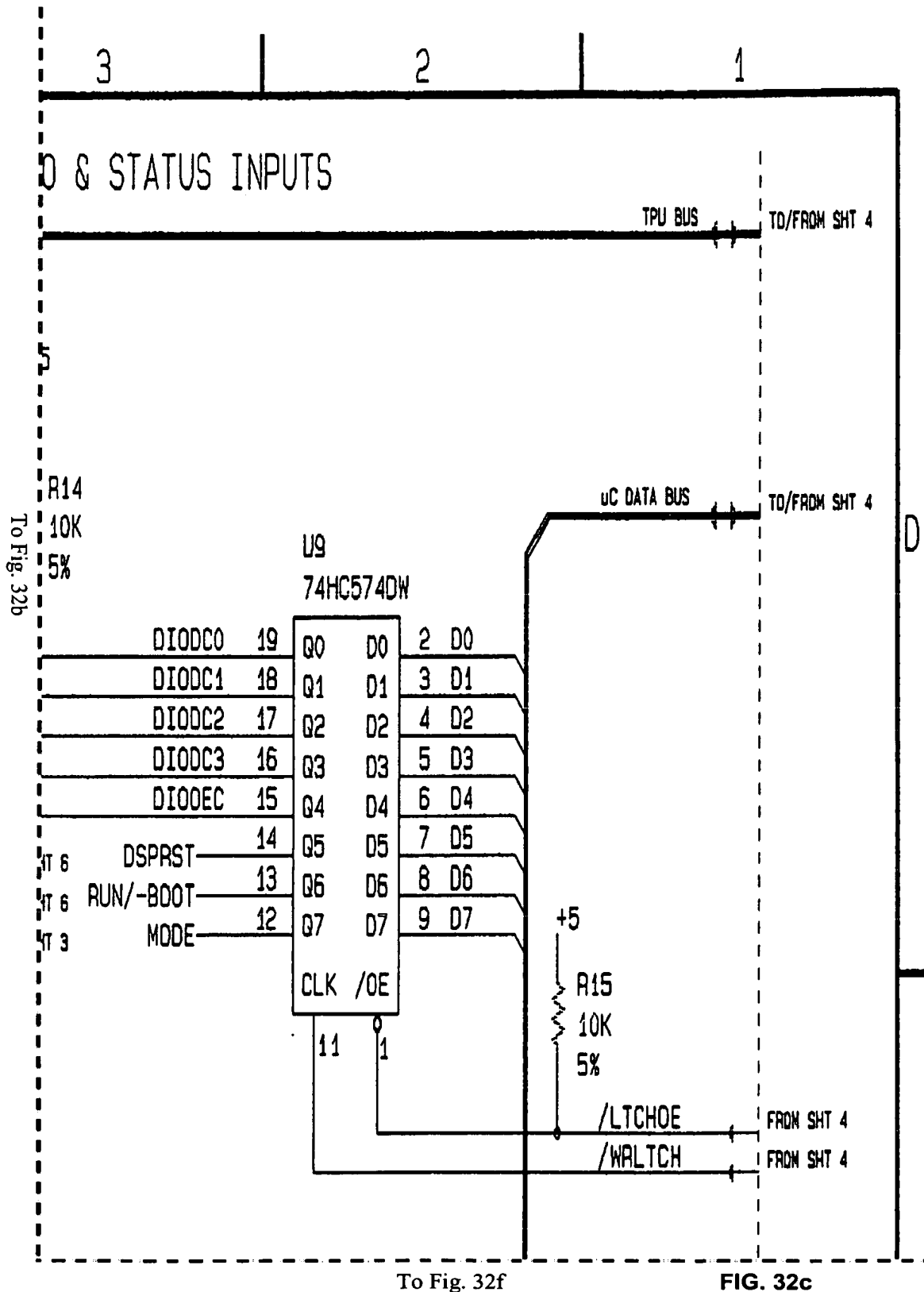
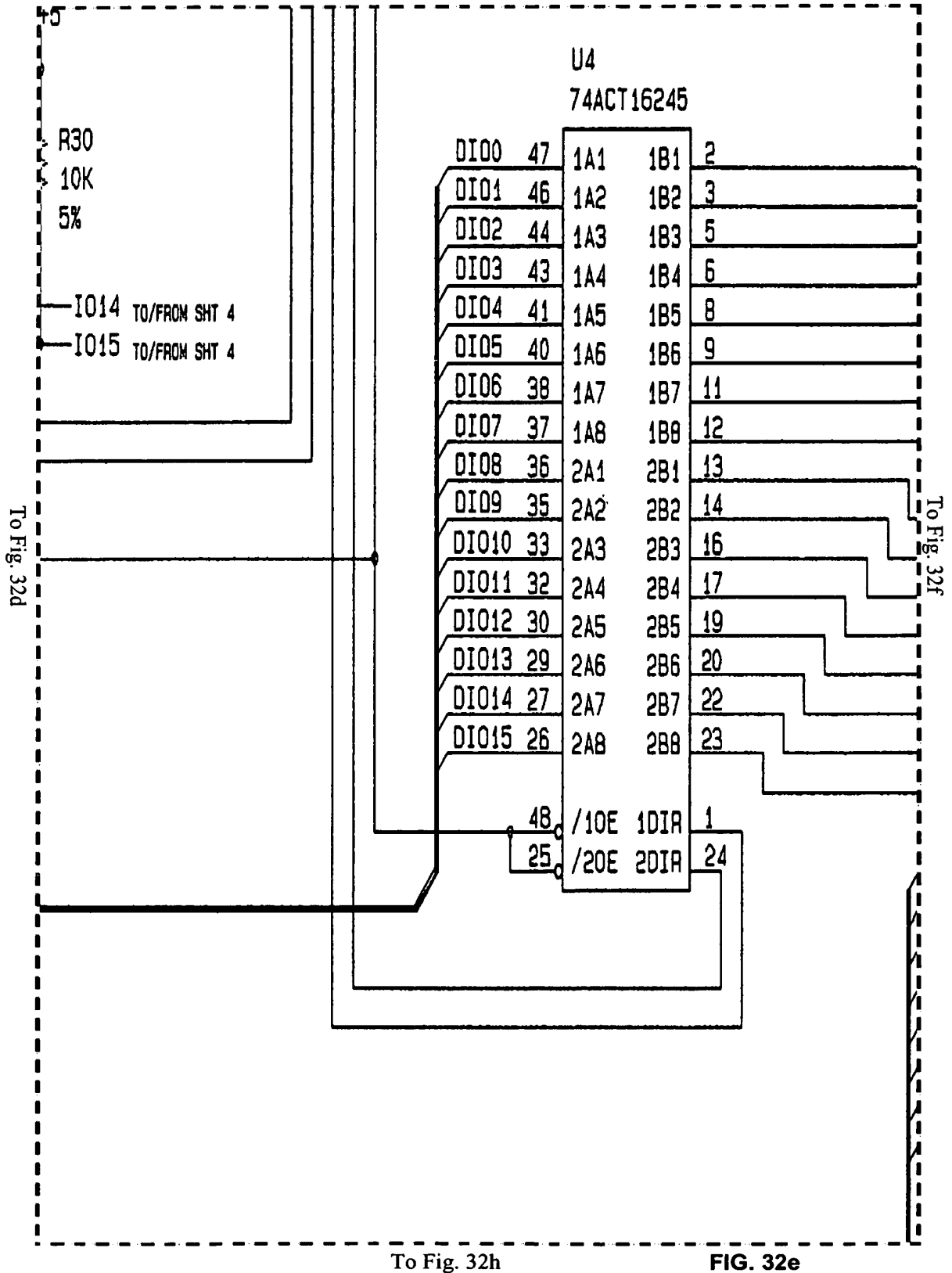
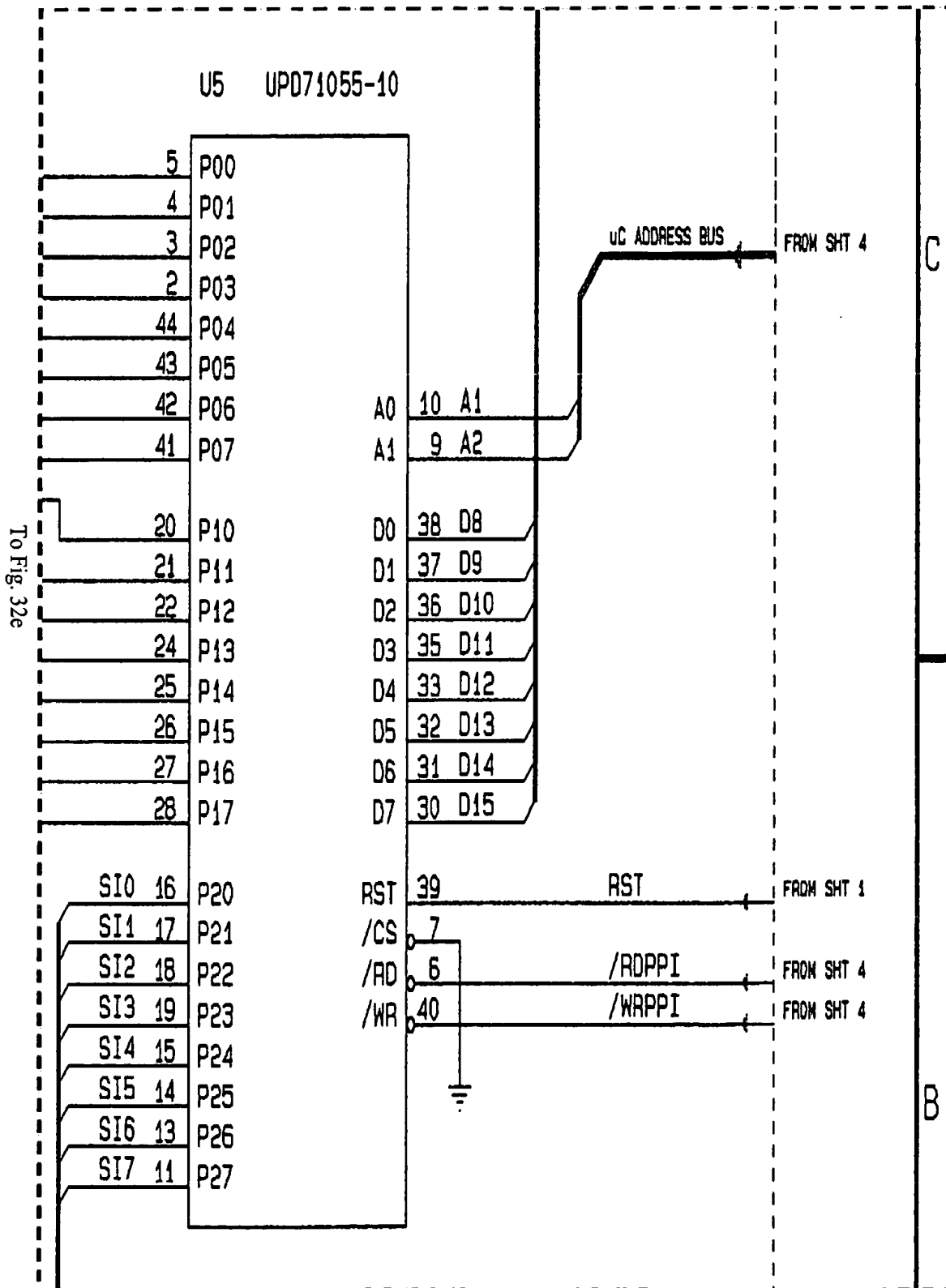


FIG. 32d

To Fig. 32b



To Fig. 32c



To Fig. 32i

FIG. 32f

To Fig. 32d

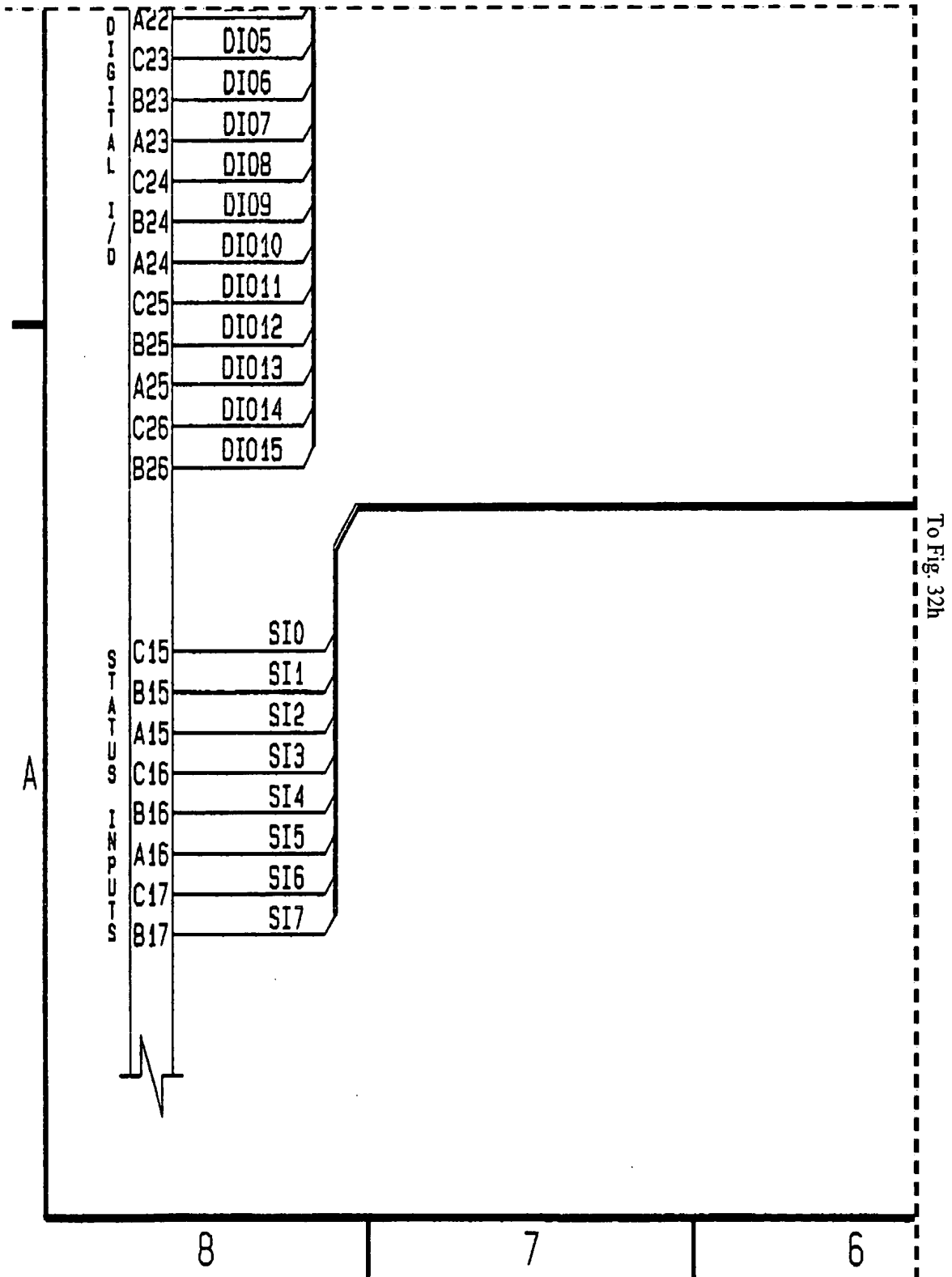


FIG. 32g



To Fig. 32e

To Fig. 32g

To Fig. 32i

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proprietary  
configuration  
are issued in  
or use shall  
of CD Power

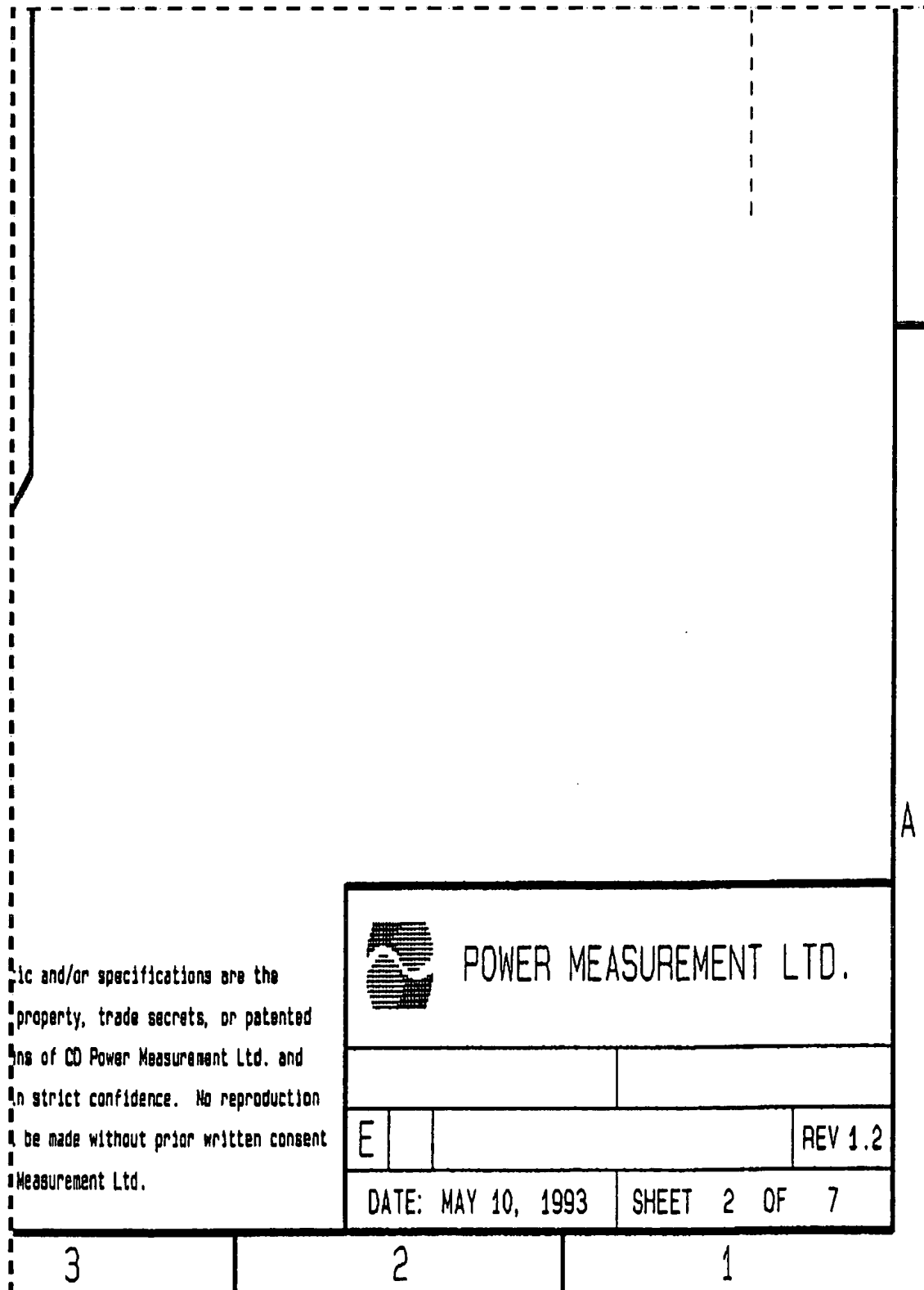
5

4


FIG. 32h

To Fig. 32f

To Fig. 32h



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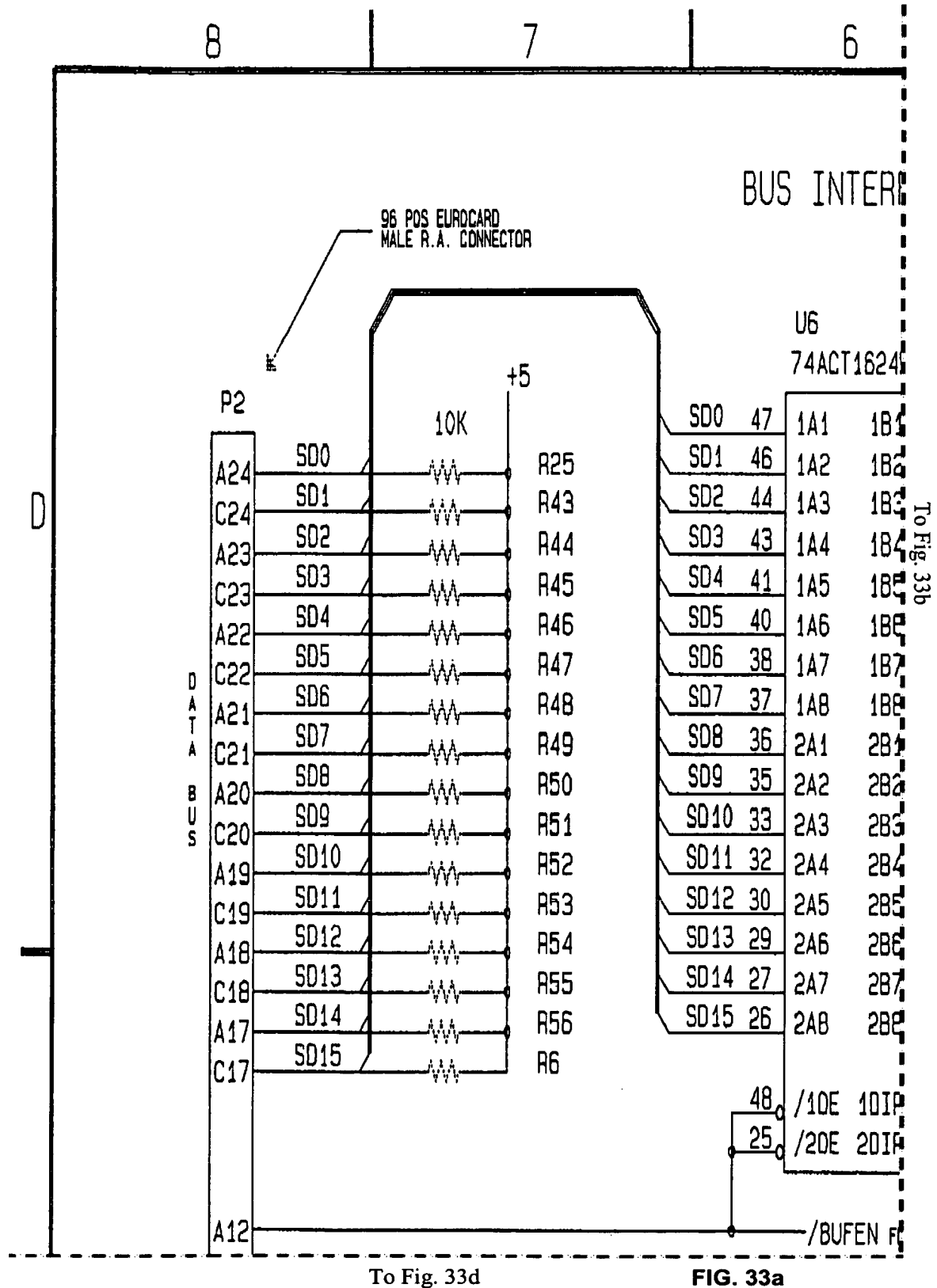
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DATE: MAY 10, 1993		SHEET 2 OF 7	

3

2

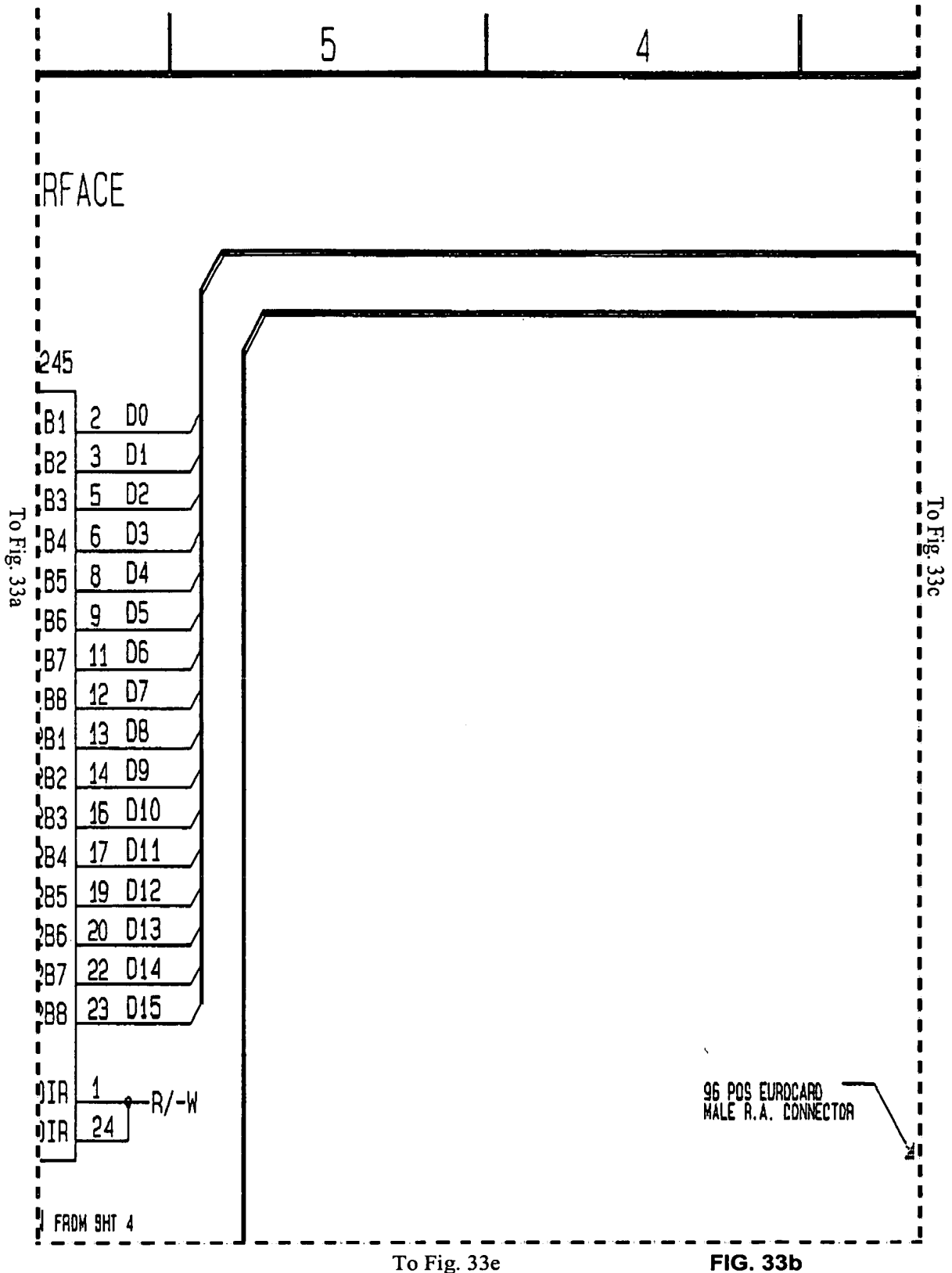
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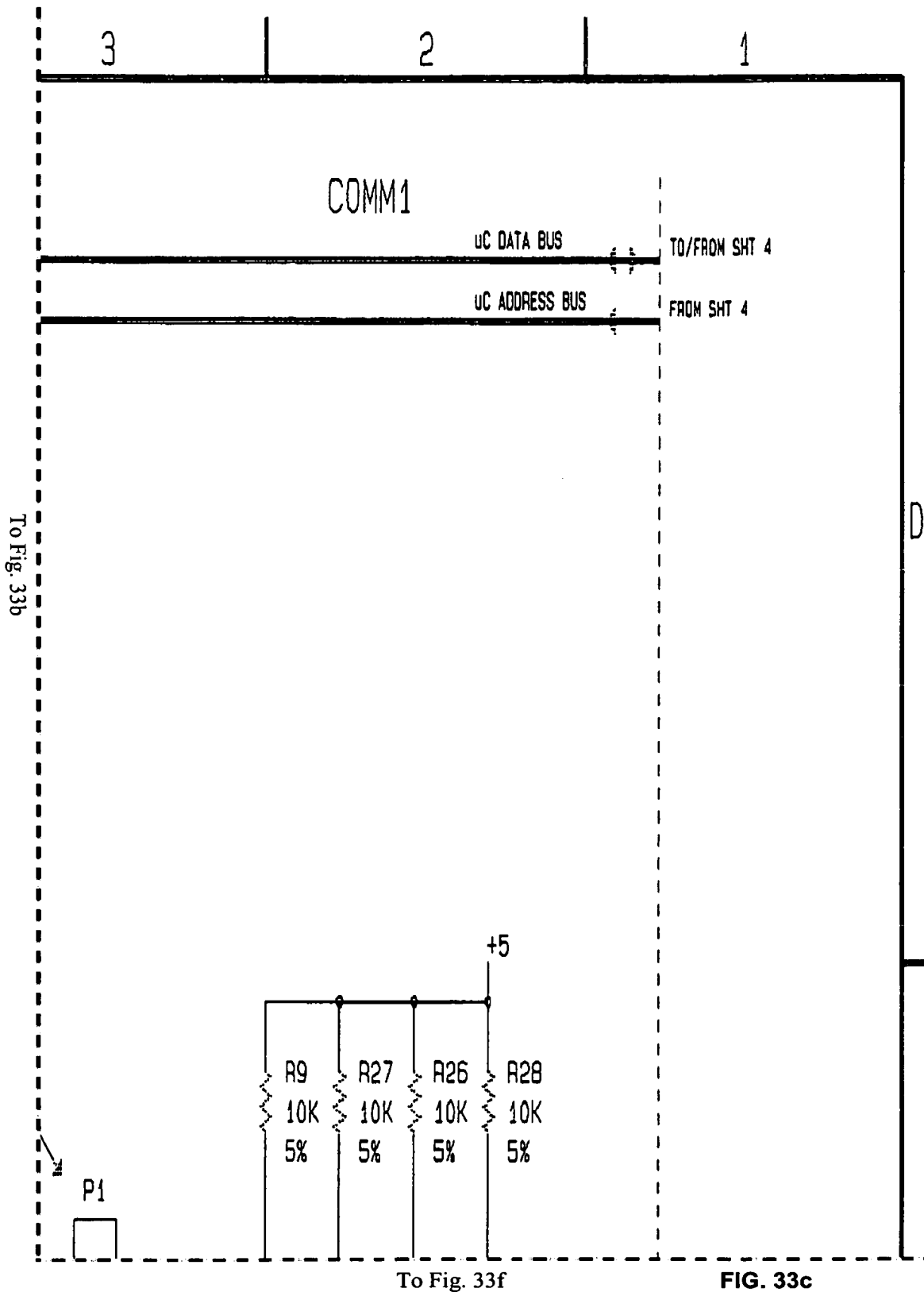
FIG. 32i



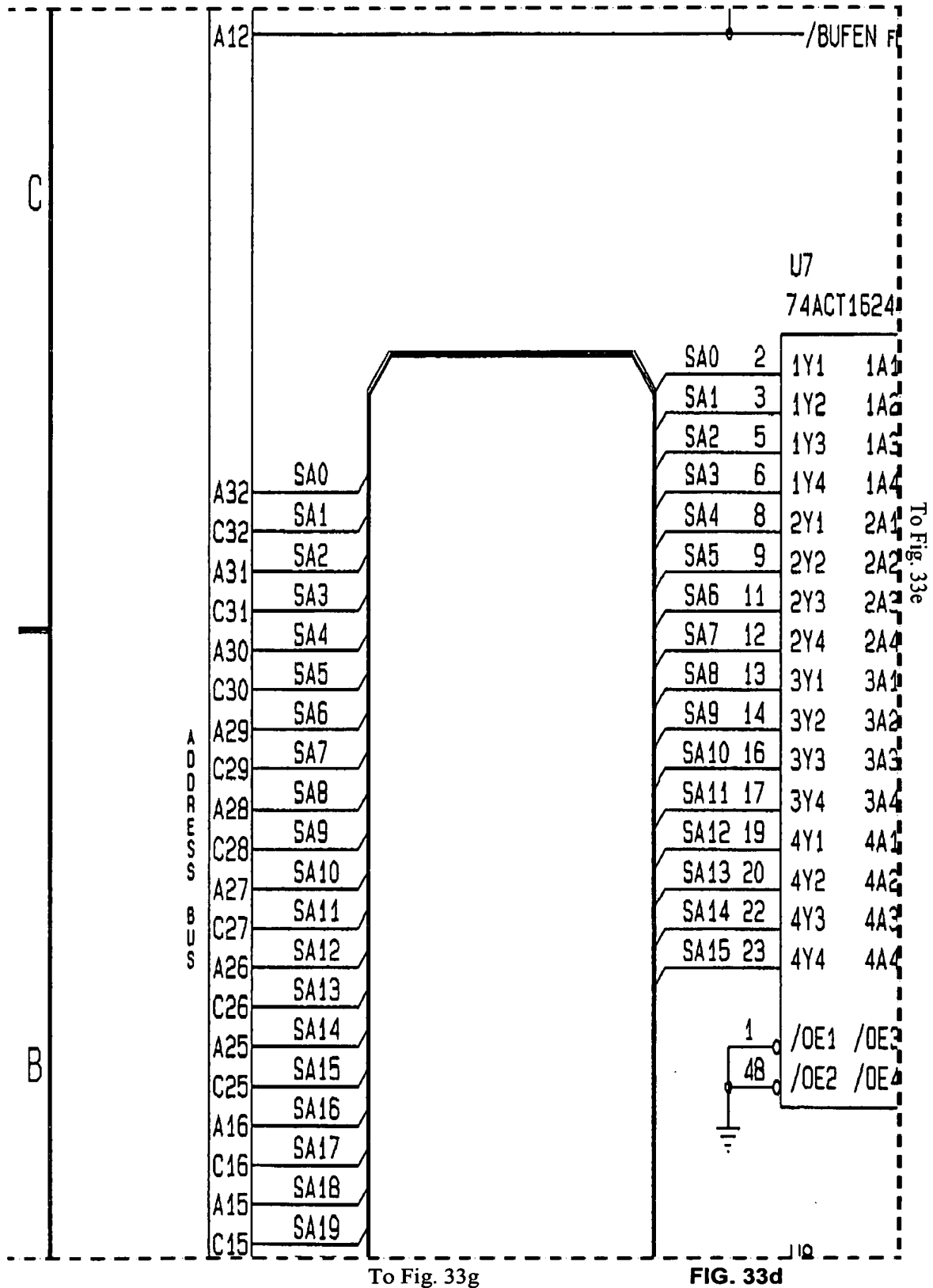
To Fig. 33d

FIG. 33a

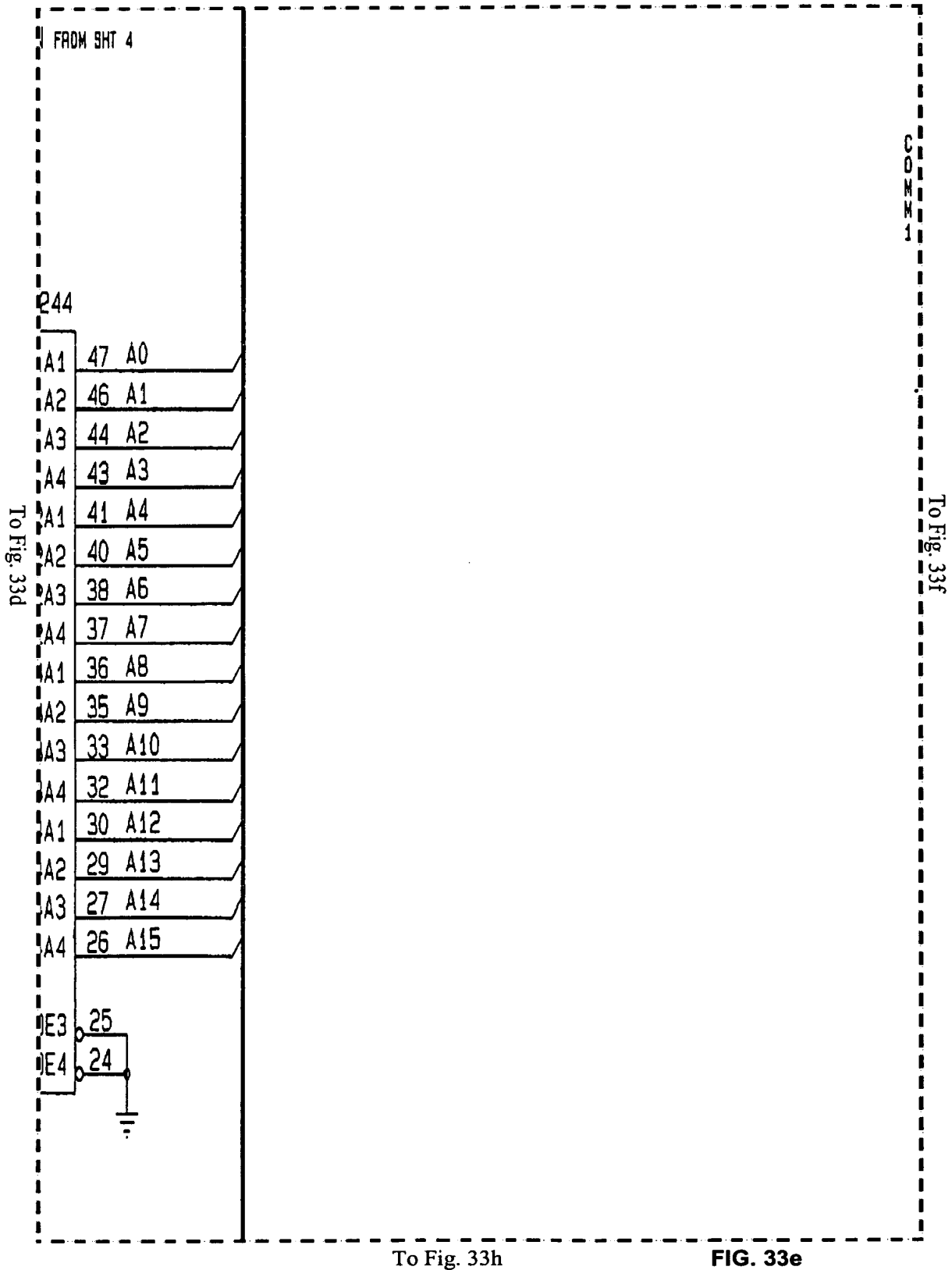




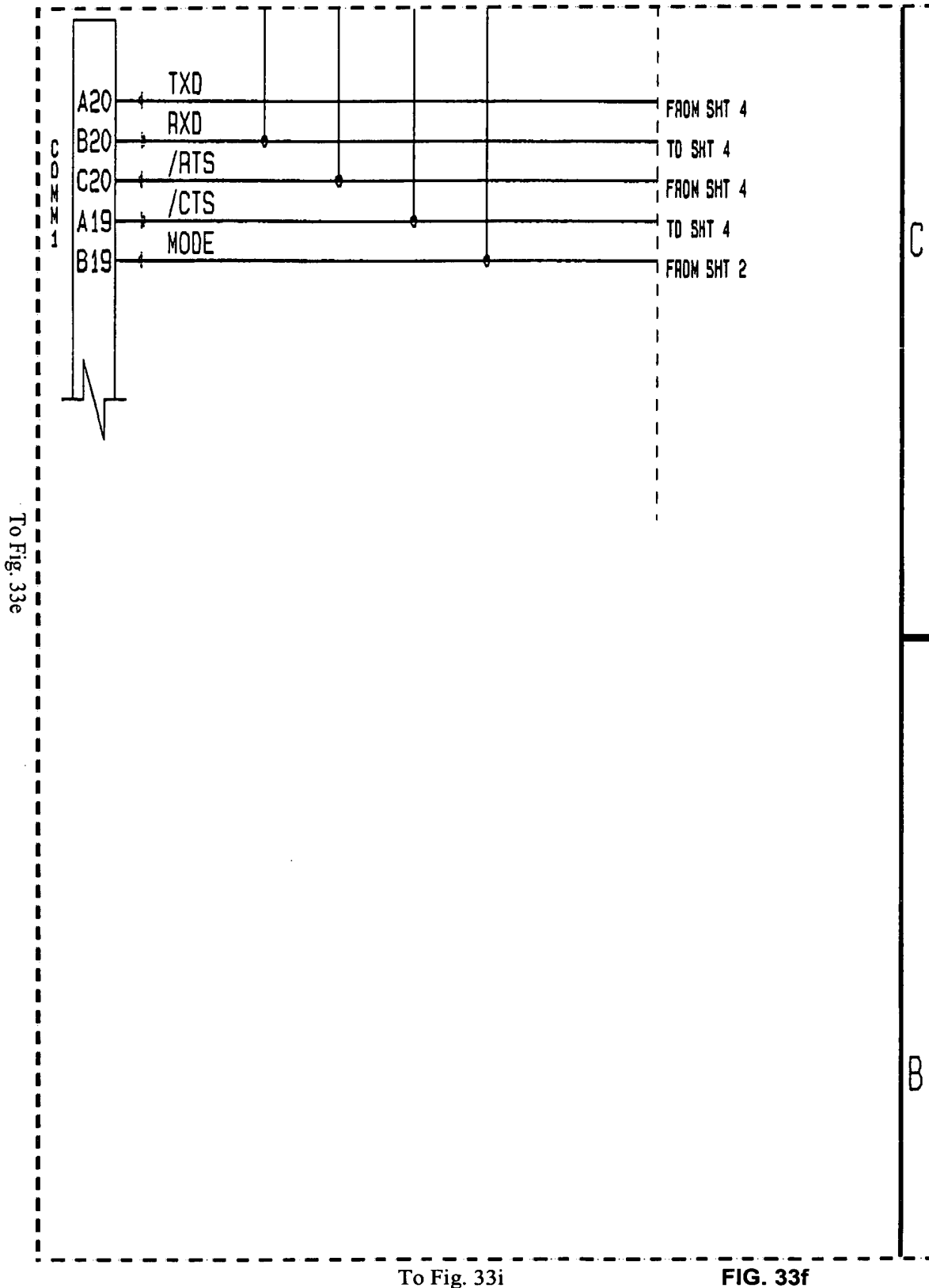
To Fig. 33a



To Fig. 33b

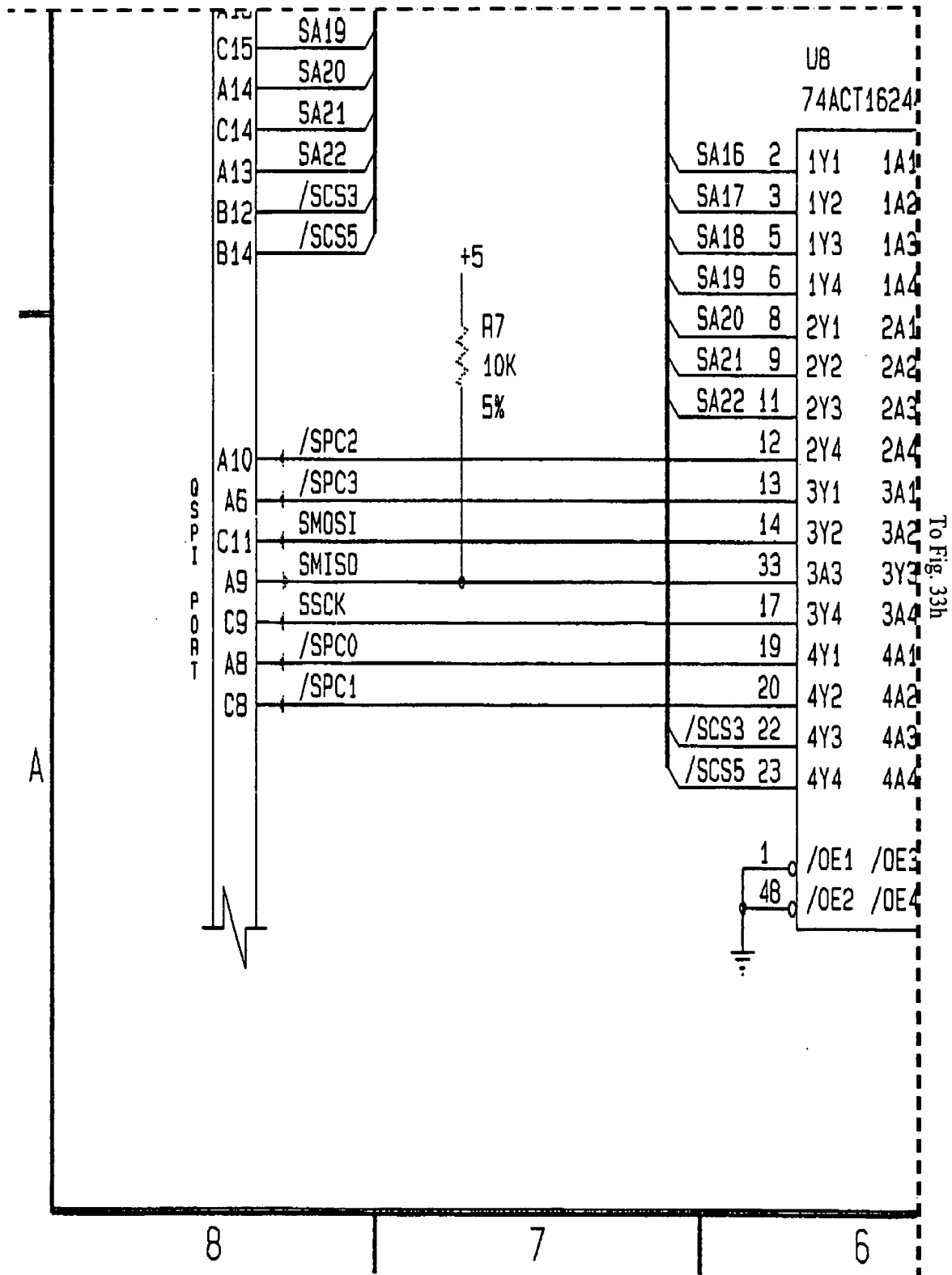


To Fig. 33c





To Fig. 33d



To Fig. 33e

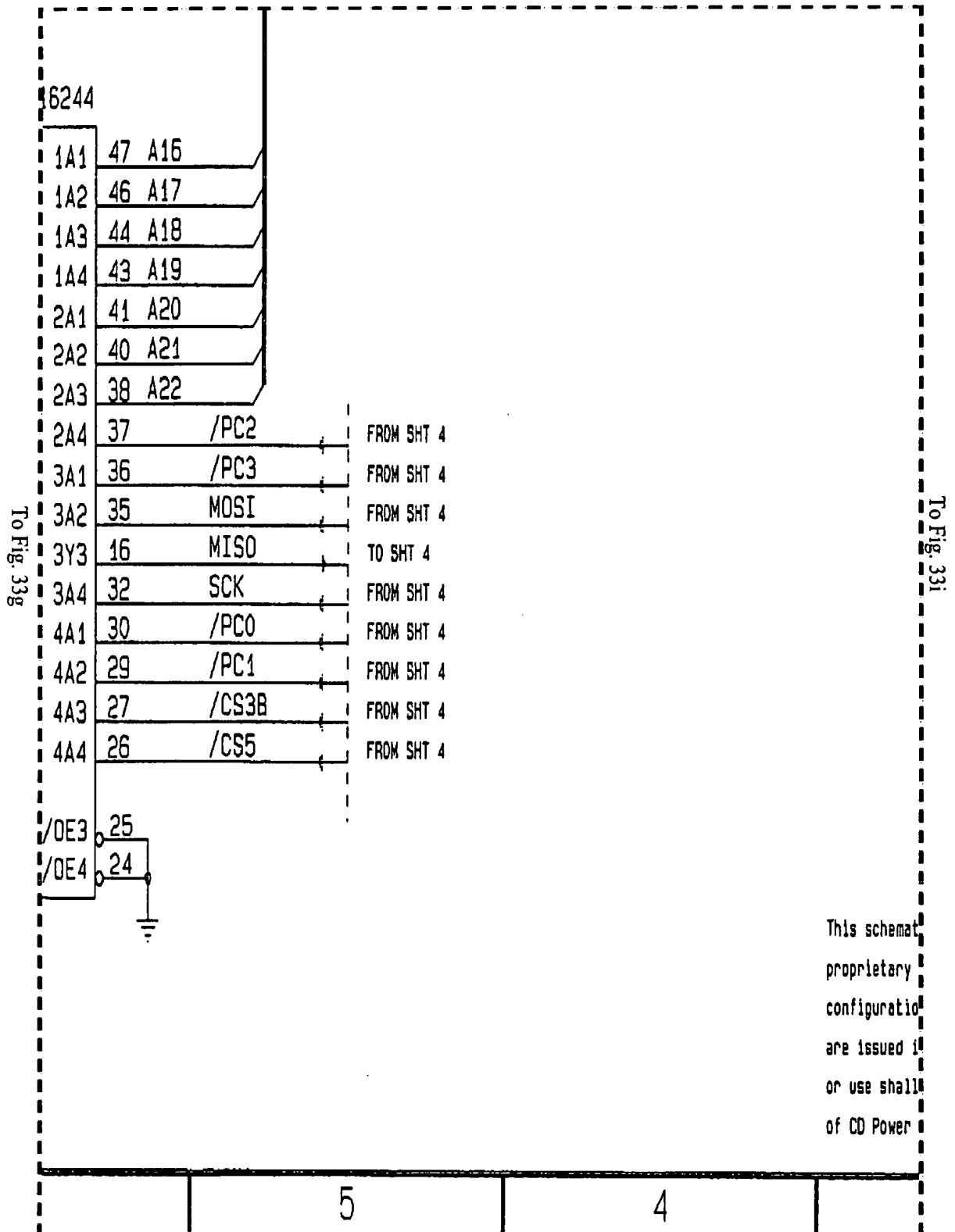
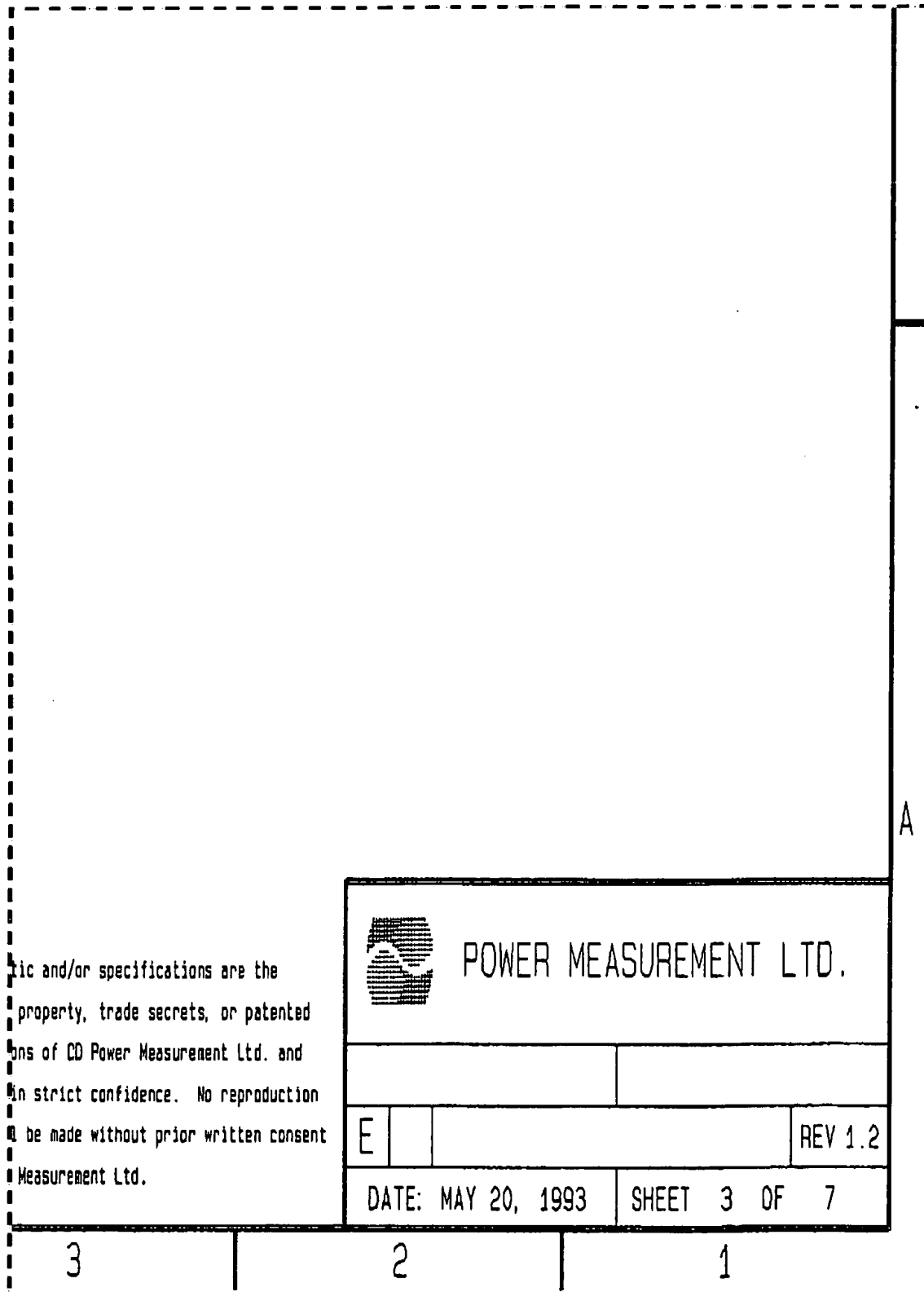


FIG. 33h

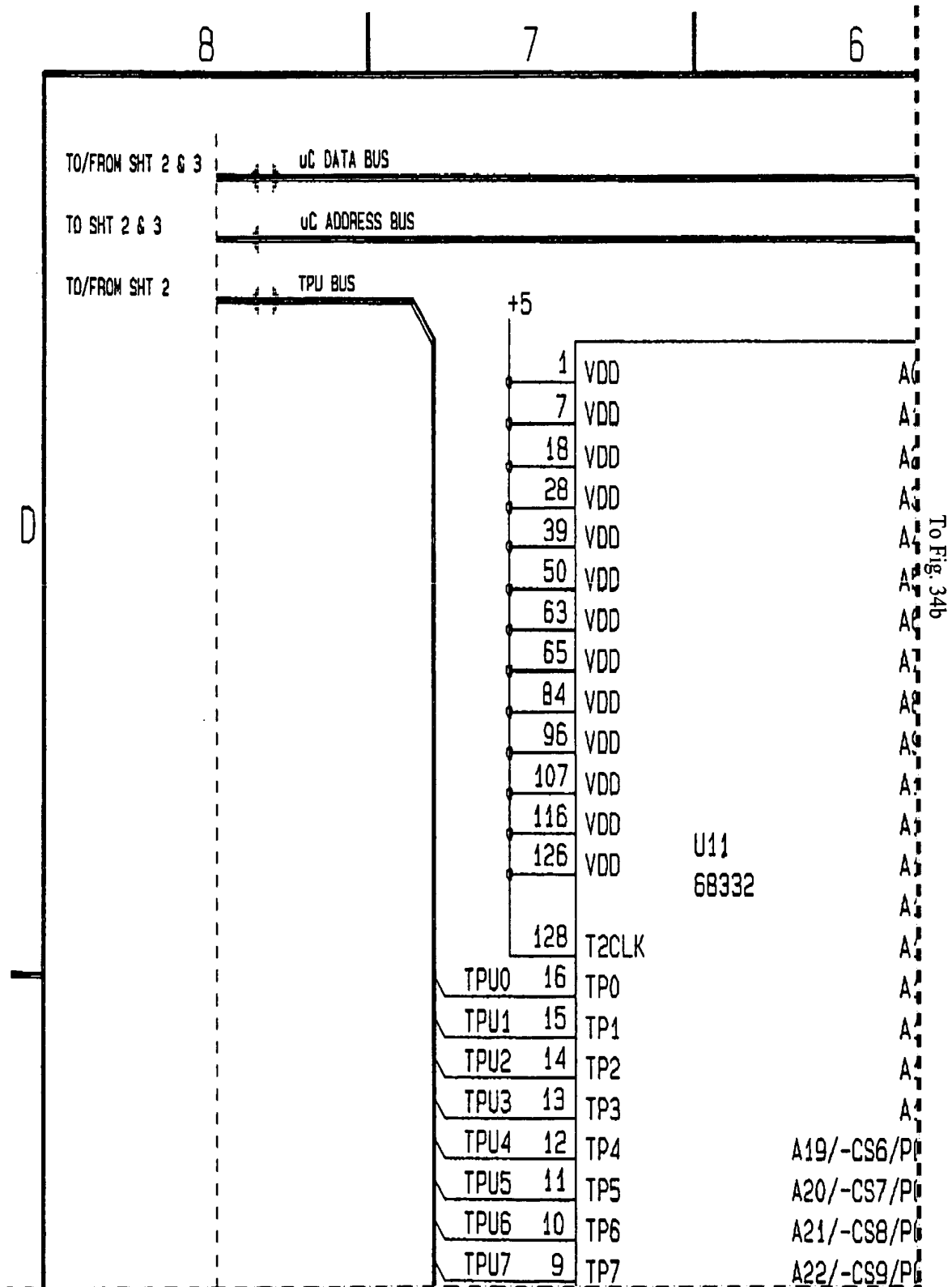
To Fig. 33f

To Fig. 33h



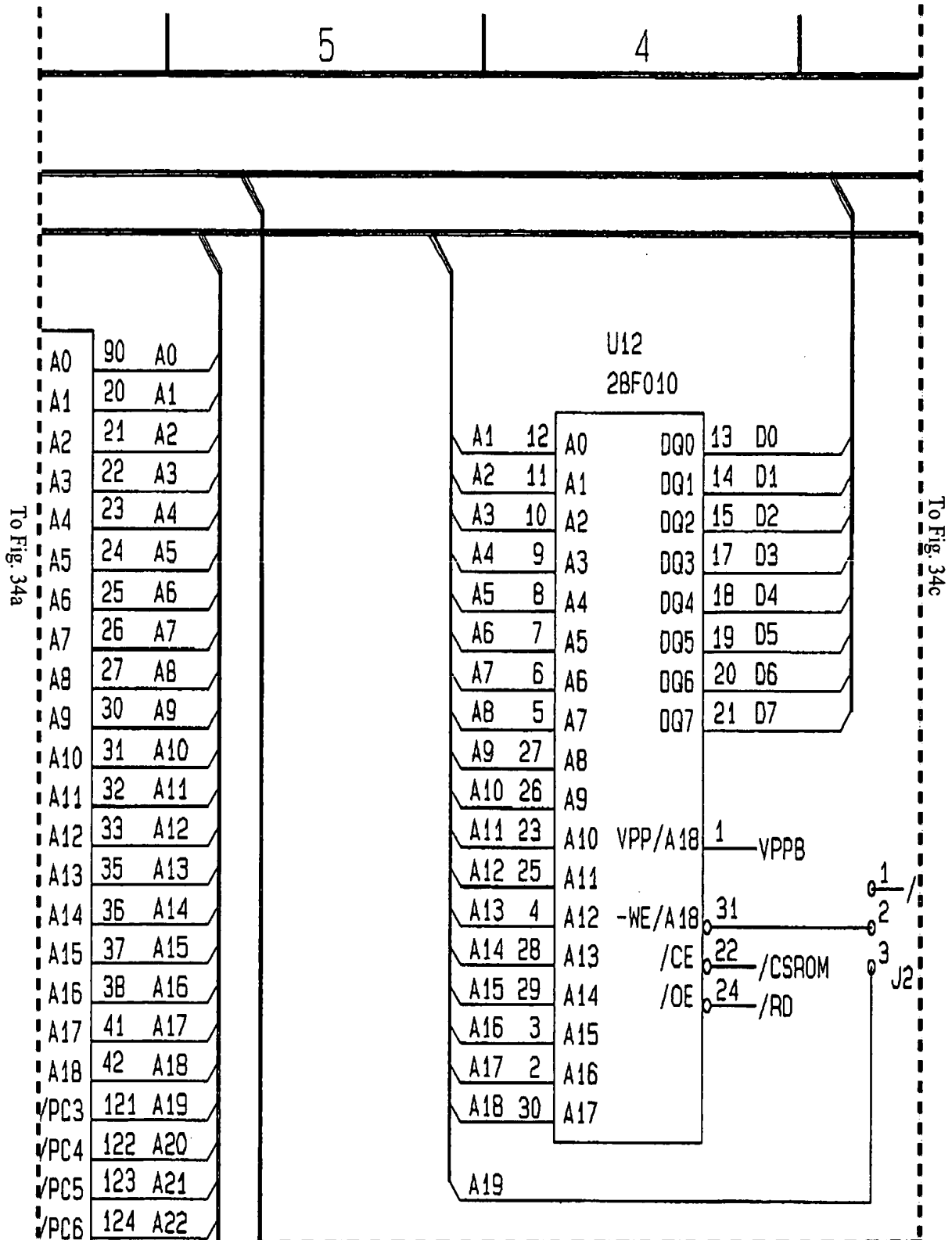
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FIG. 33i



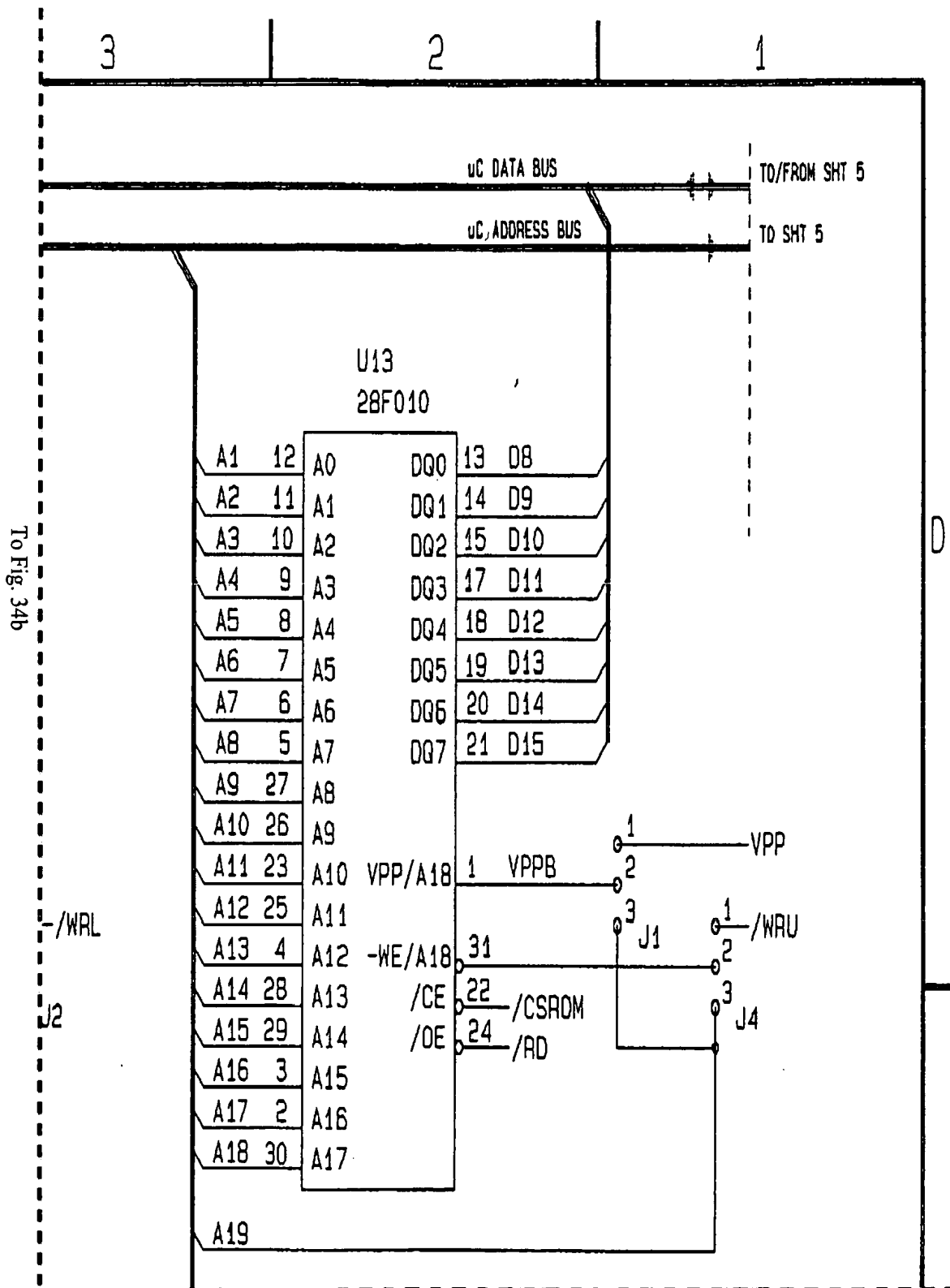
To Fig. 34d

FIG. 34a



To Fig. 34e

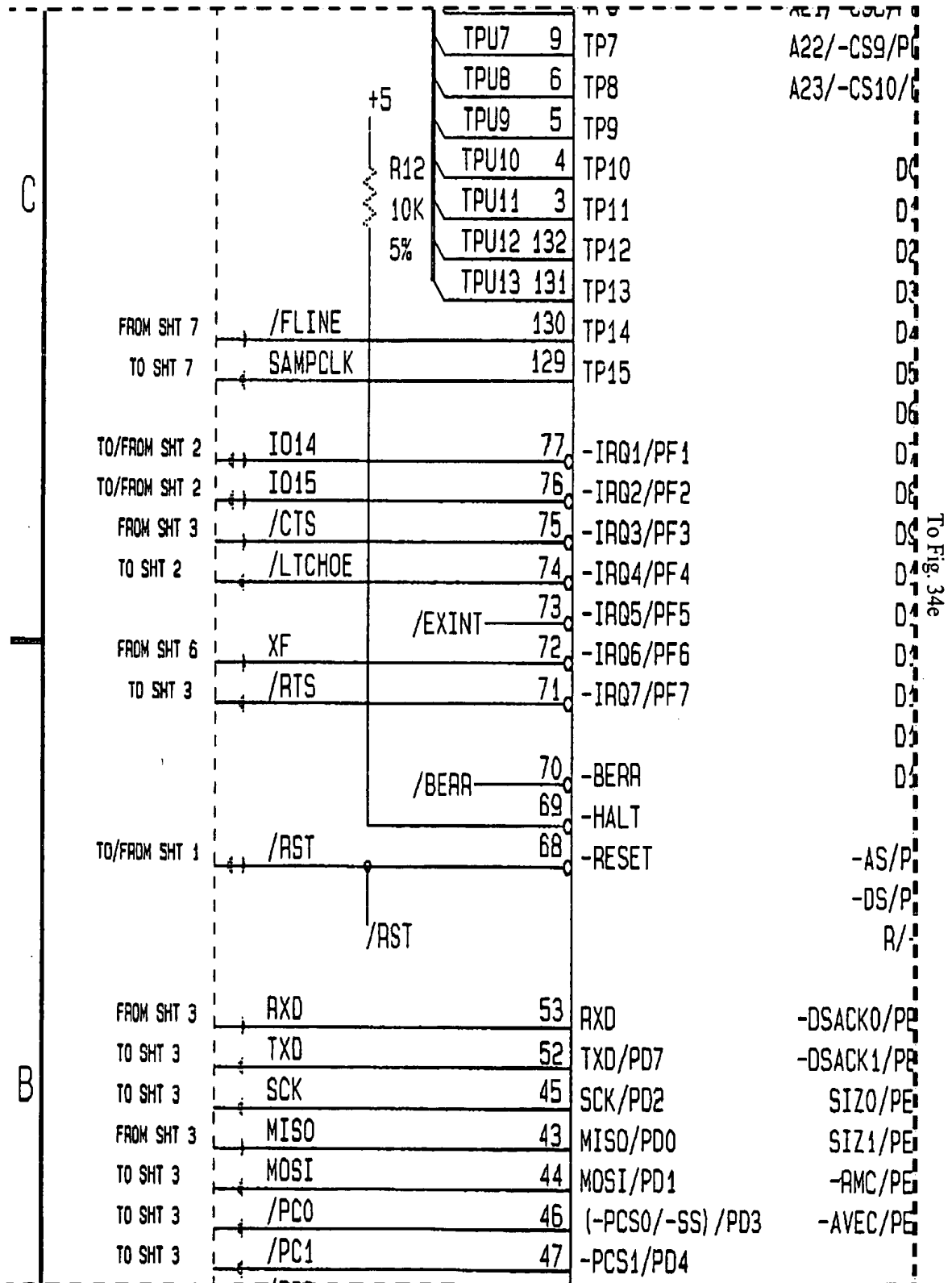
FIG. 34b



To Fig. 34f

FIG. 34c

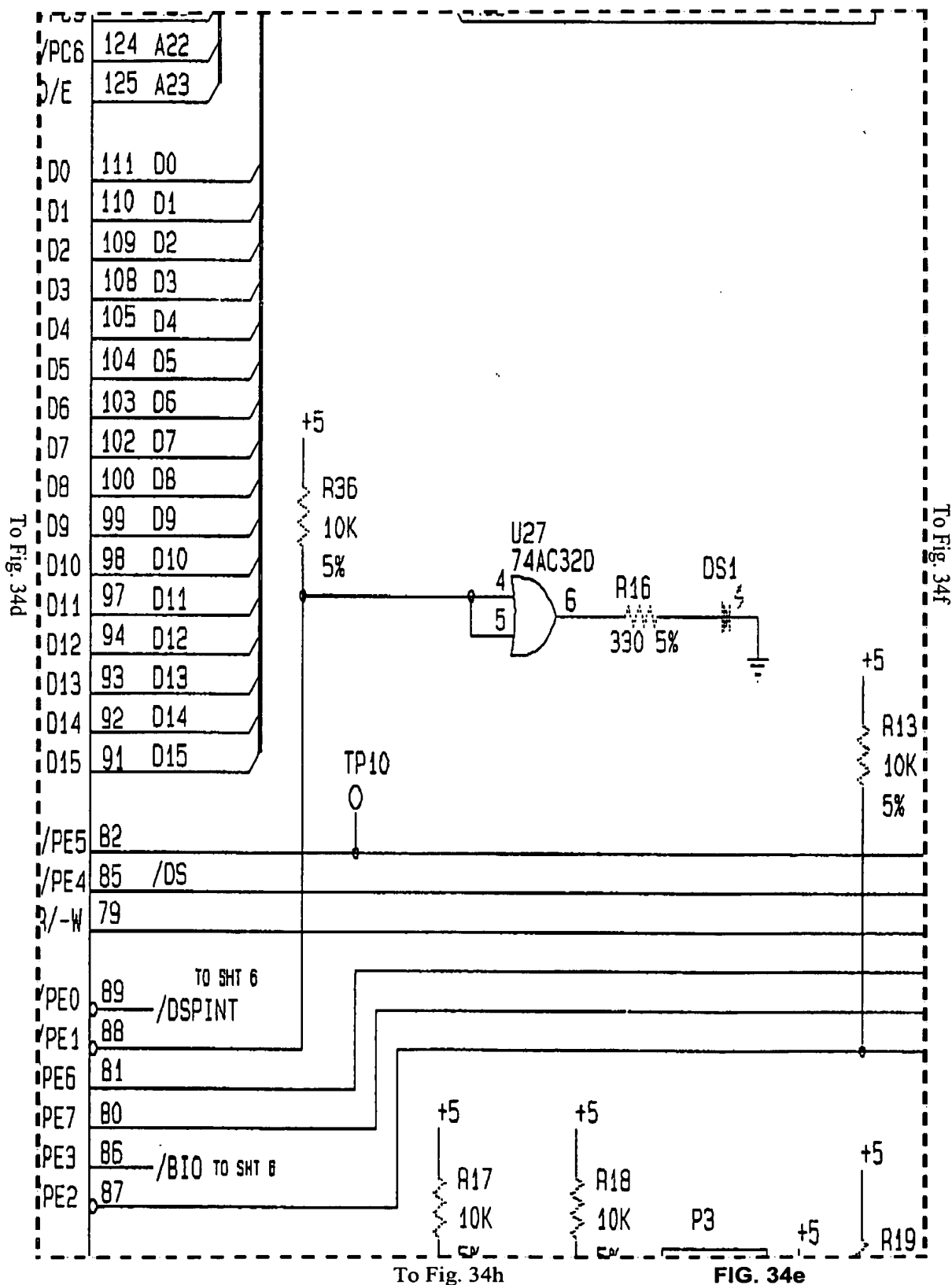
To Fig. 34a



To Fig. 34g

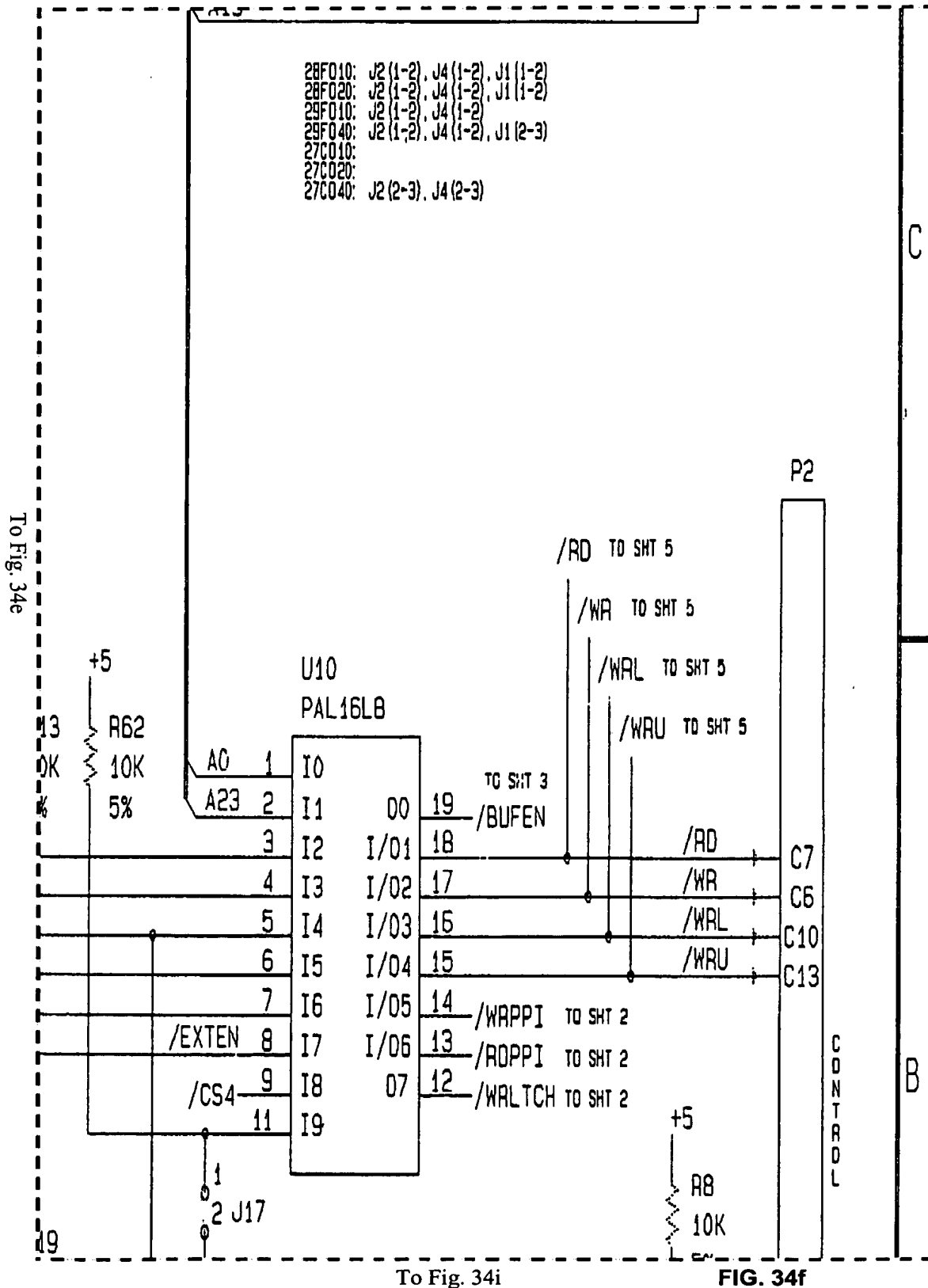
FIG. 34d

To Fig. 34b





To Fig. 34c



To Fig. 34d

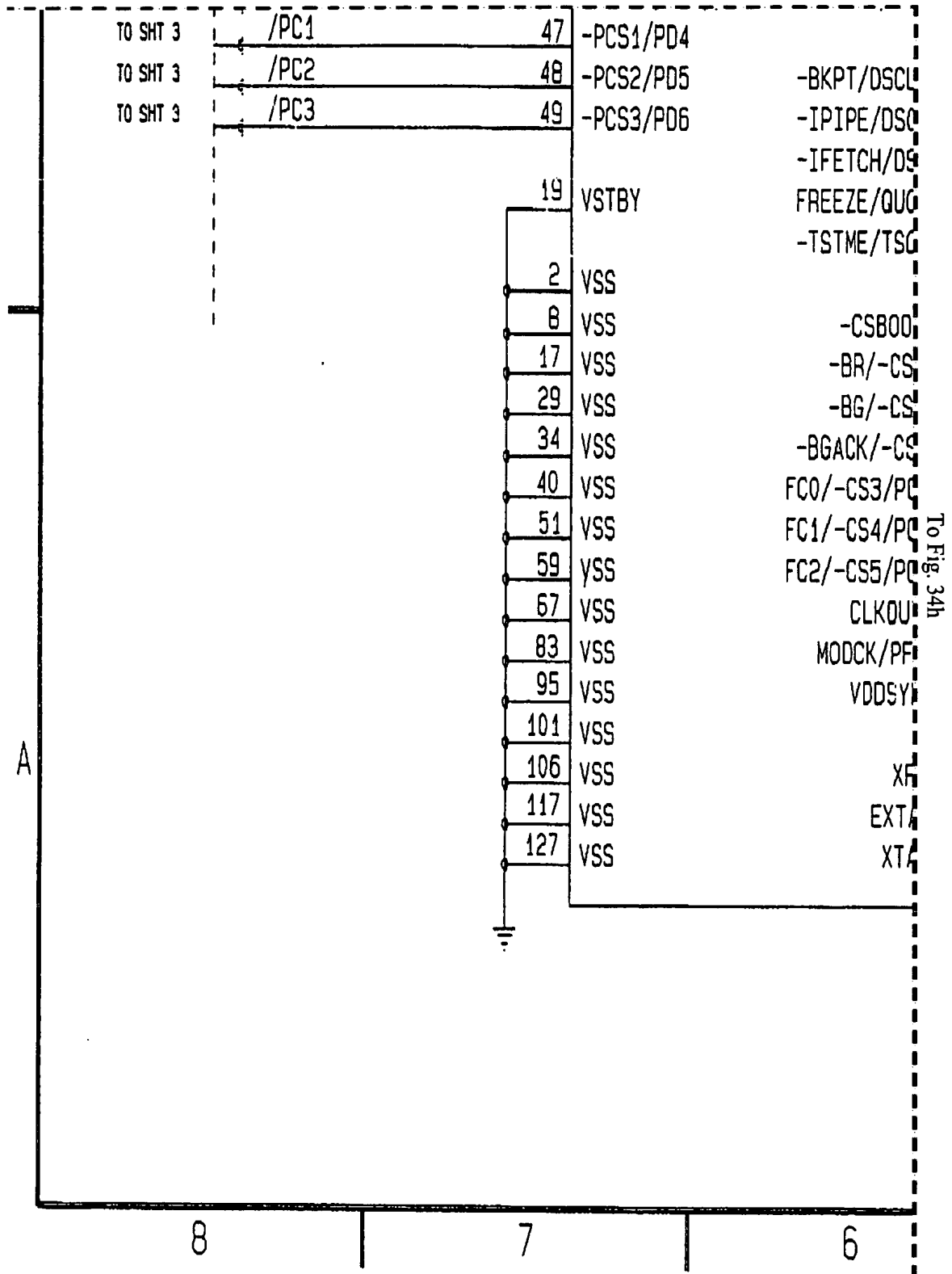


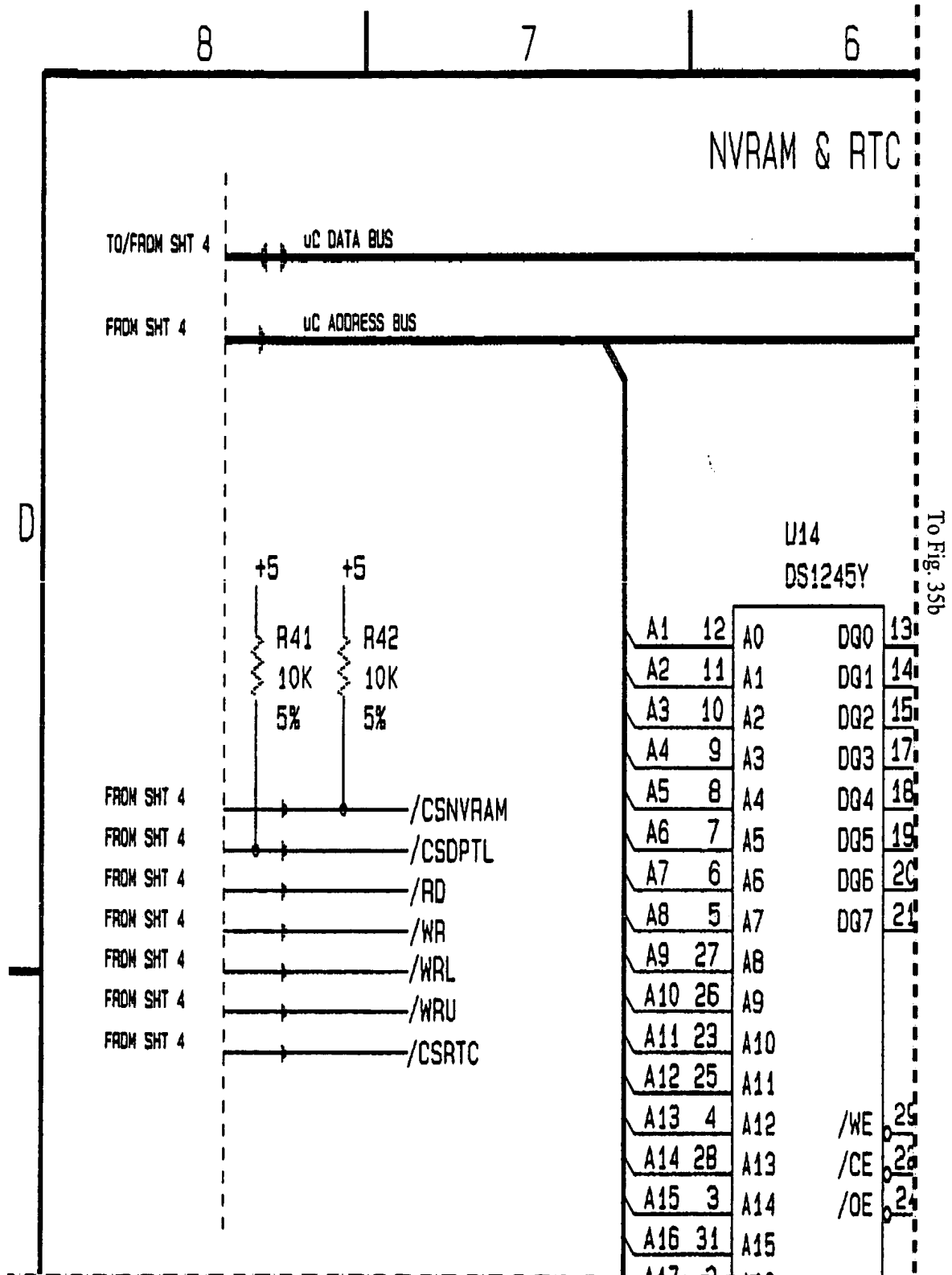
FIG. 34g



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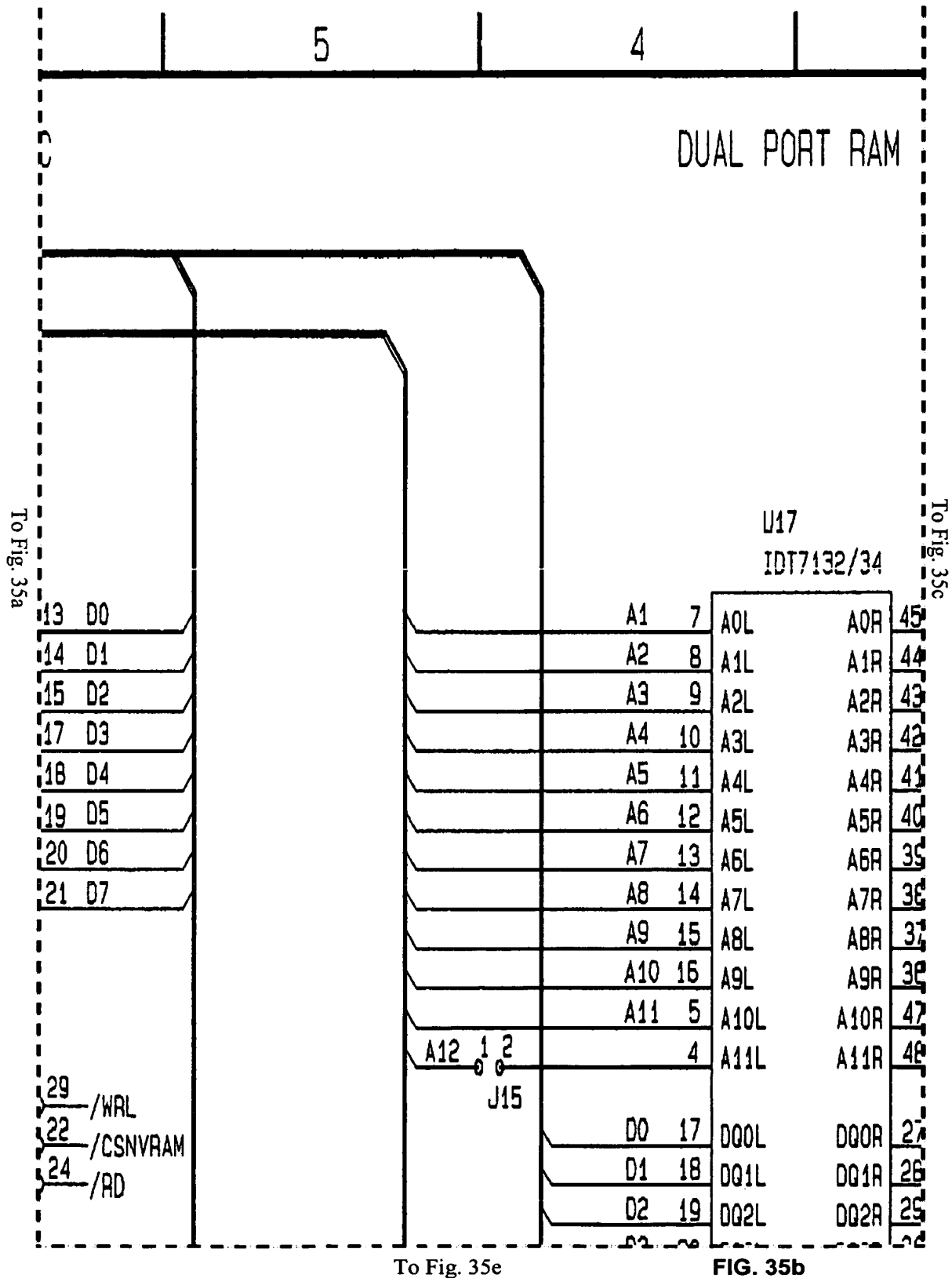
3 2 1

**FIG. 34i**



To Fig. 35d

FIG. 35a



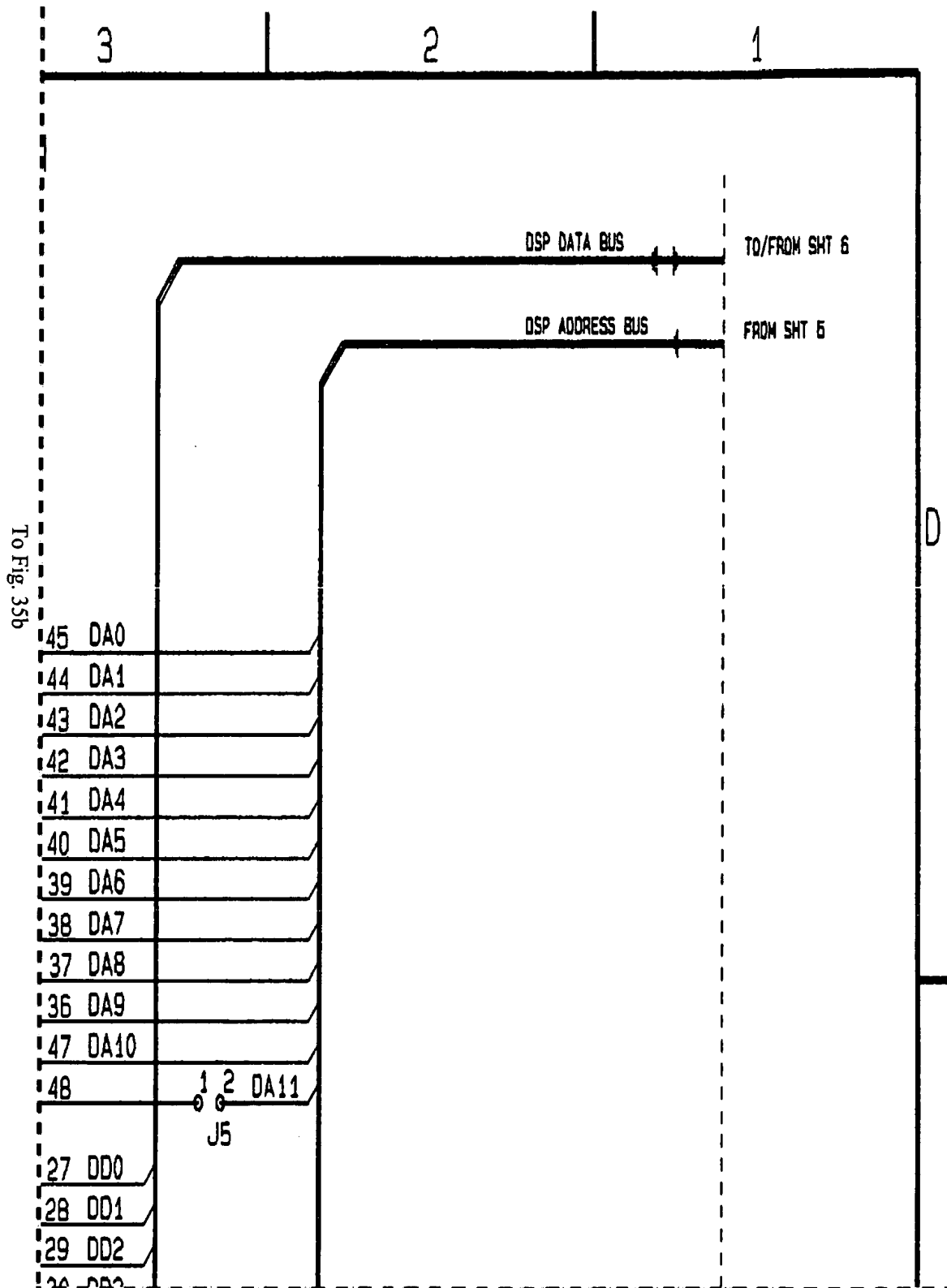
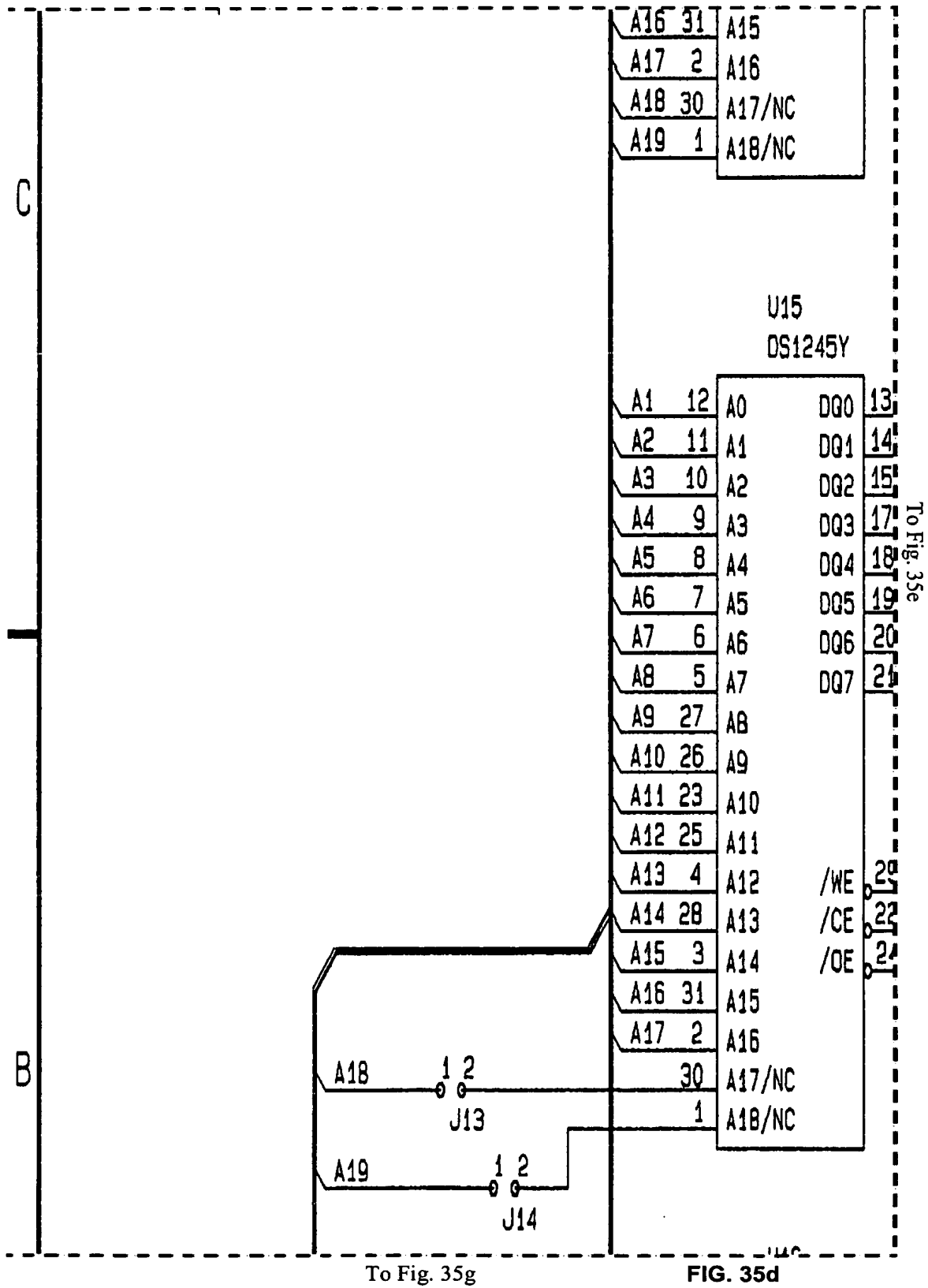


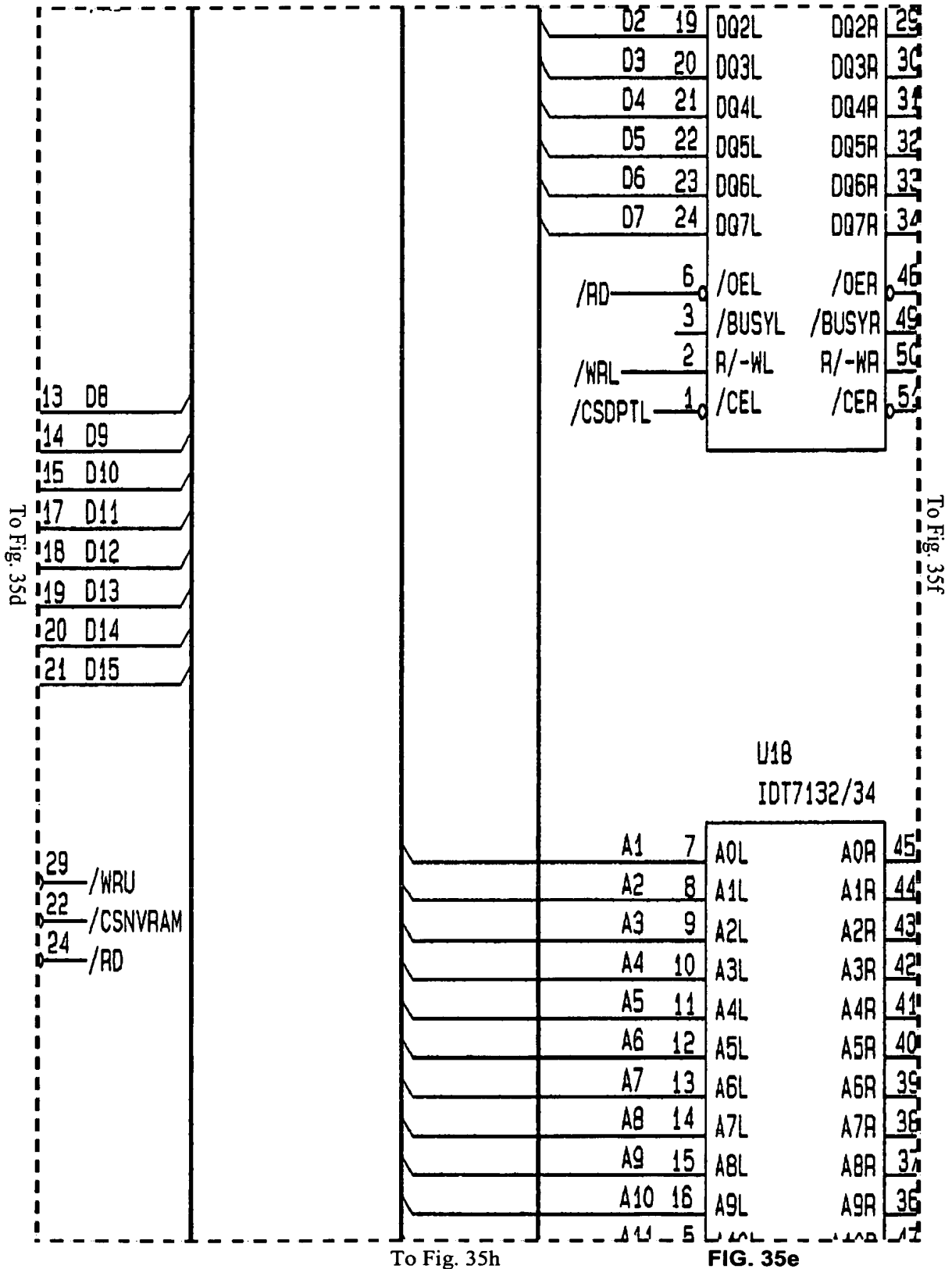
FIG. 35c

To Fig. 35a





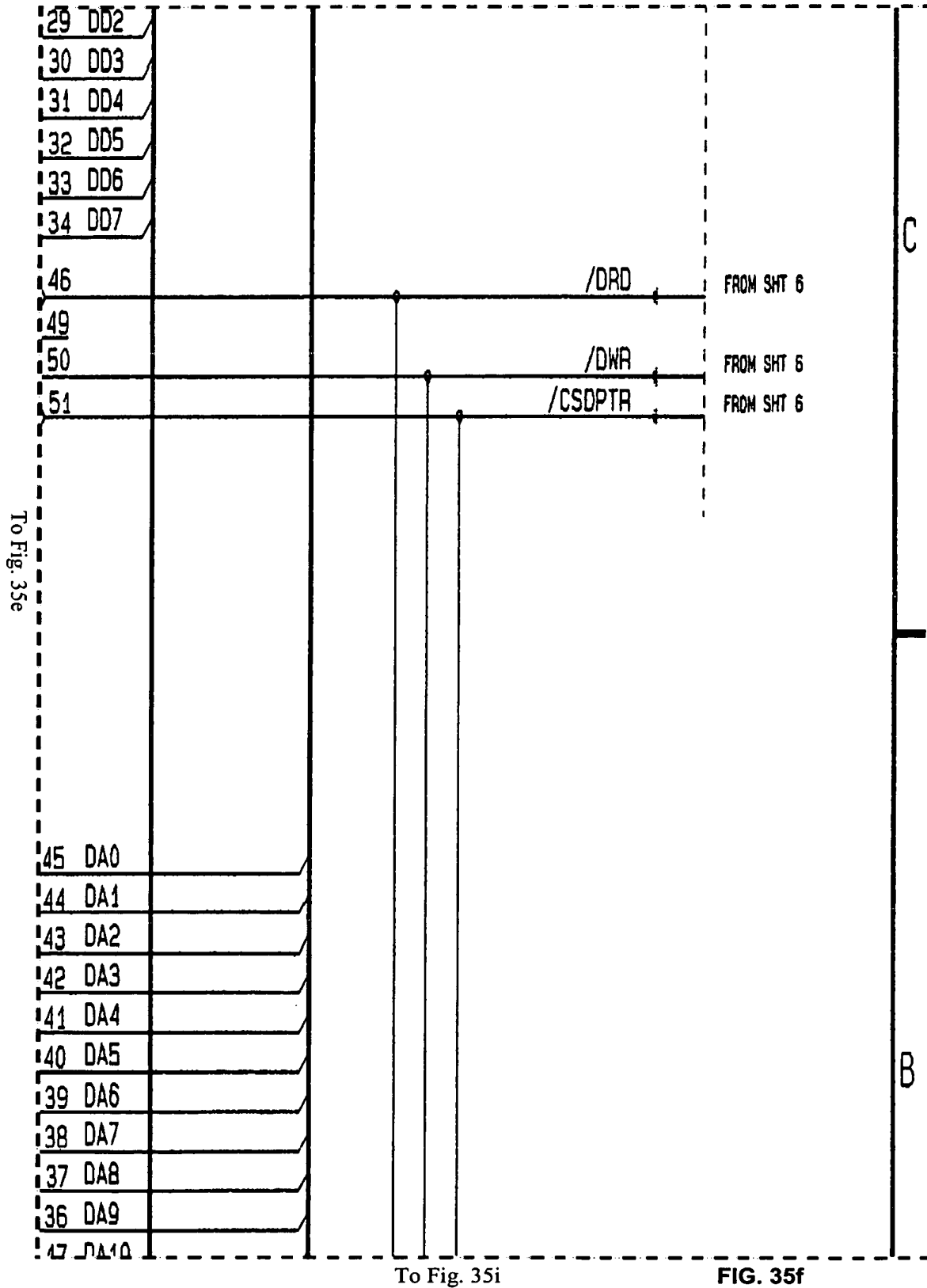
To Fig. 35b



To Fig. 35h

FIG. 35e

To Fig. 35c



To Fig. 35i

FIG. 35f

To Fig. 35d

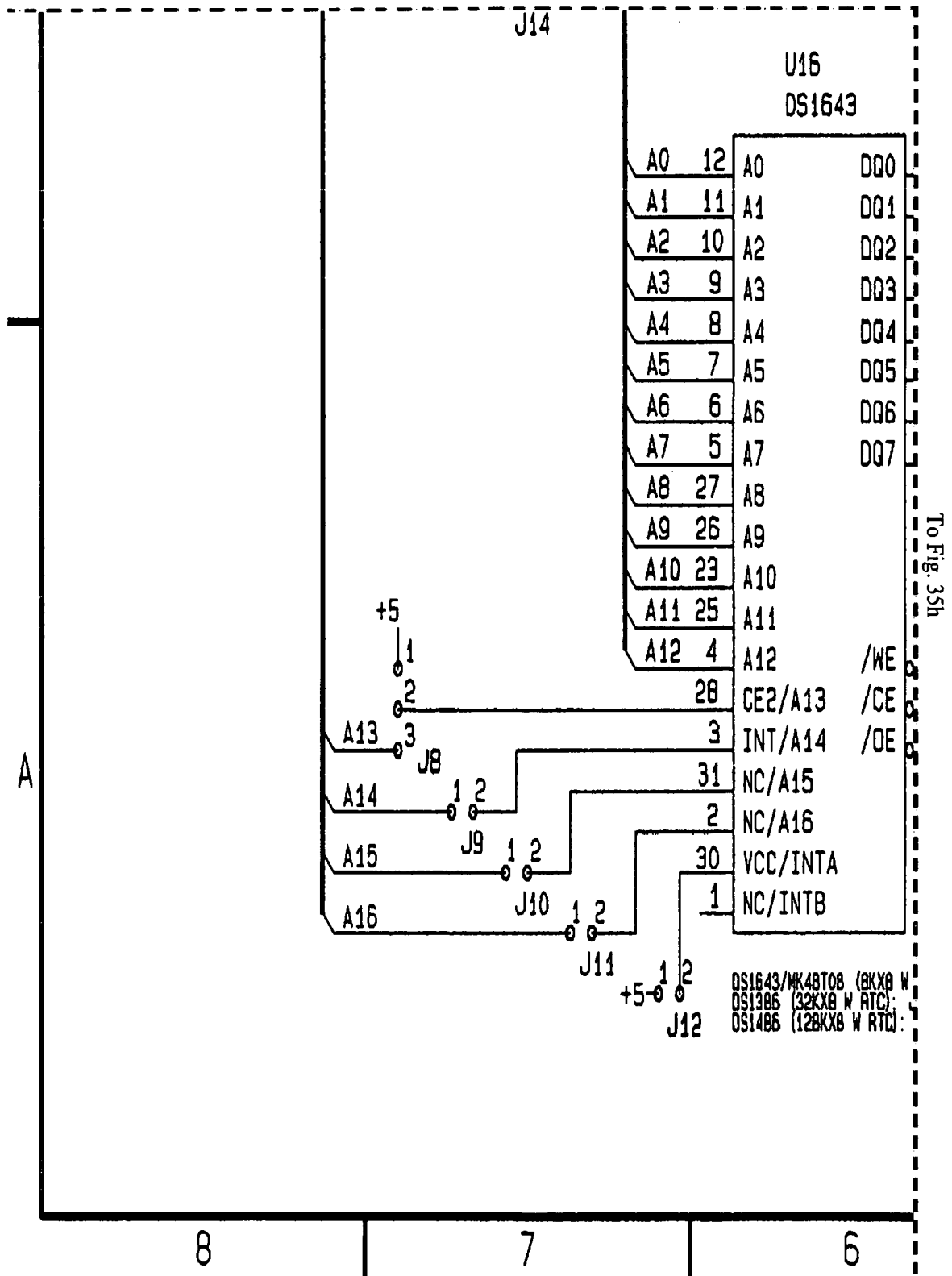


FIG. 35g

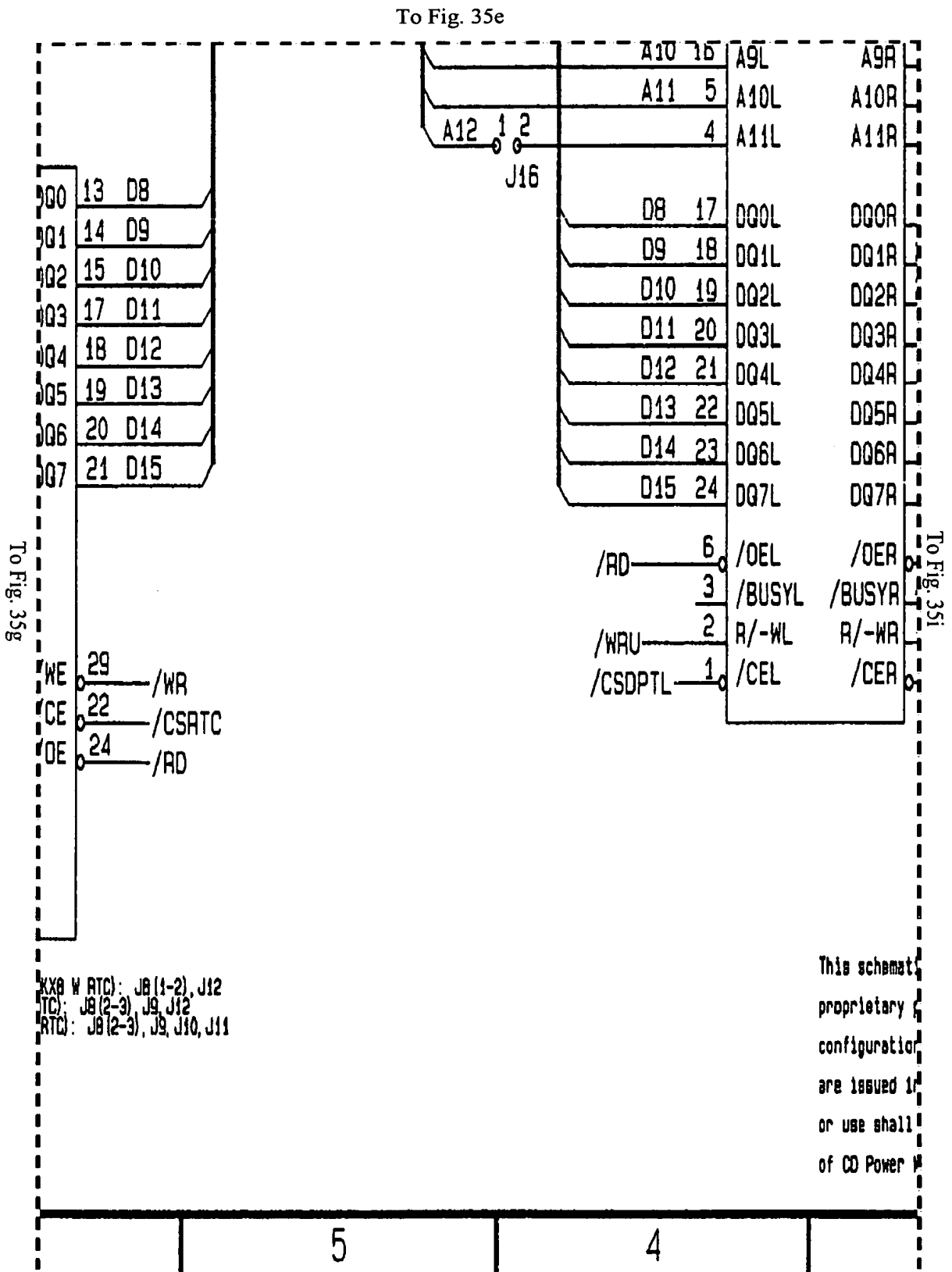
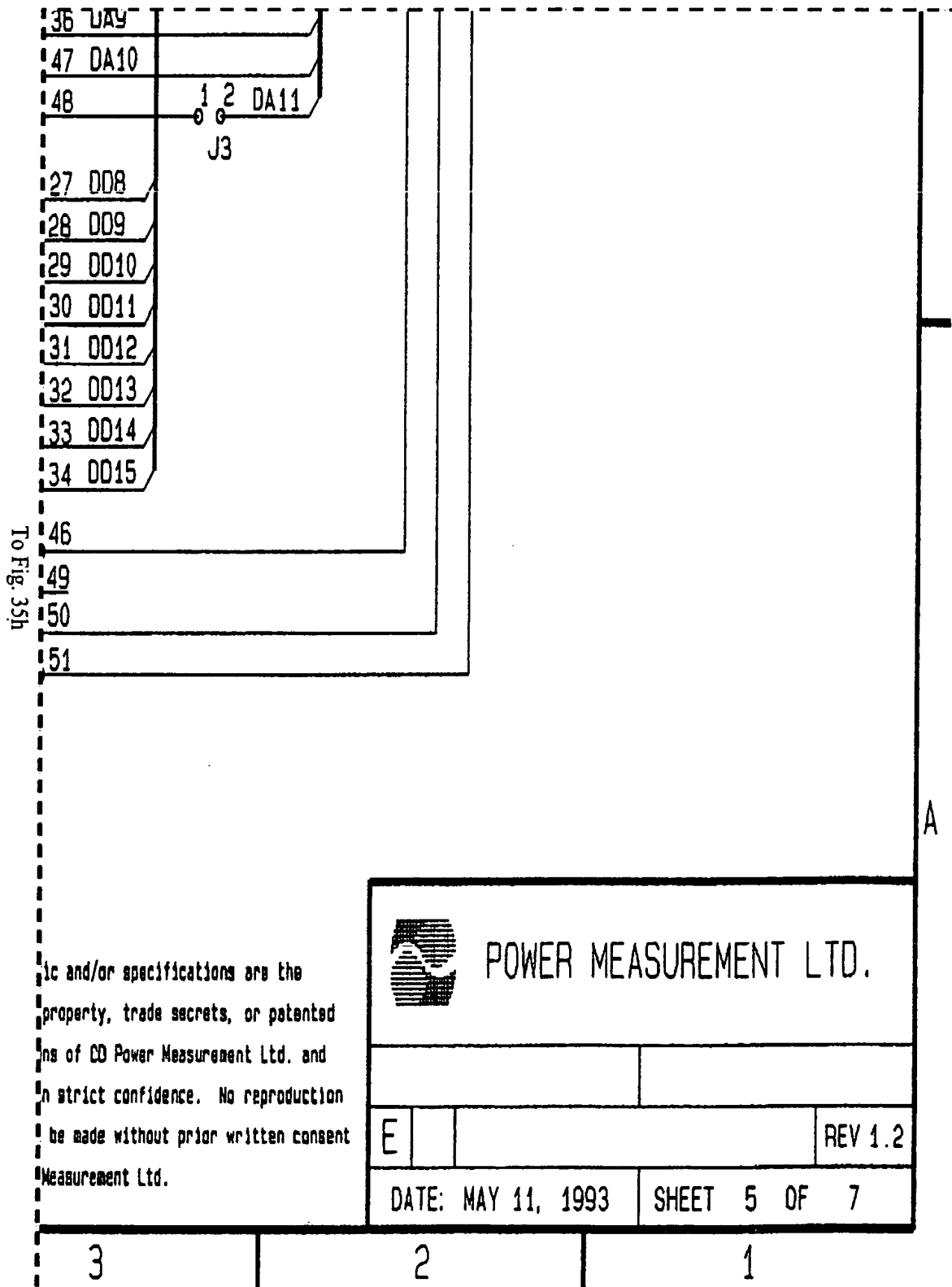


FIG. 35h

To Fig. 35f



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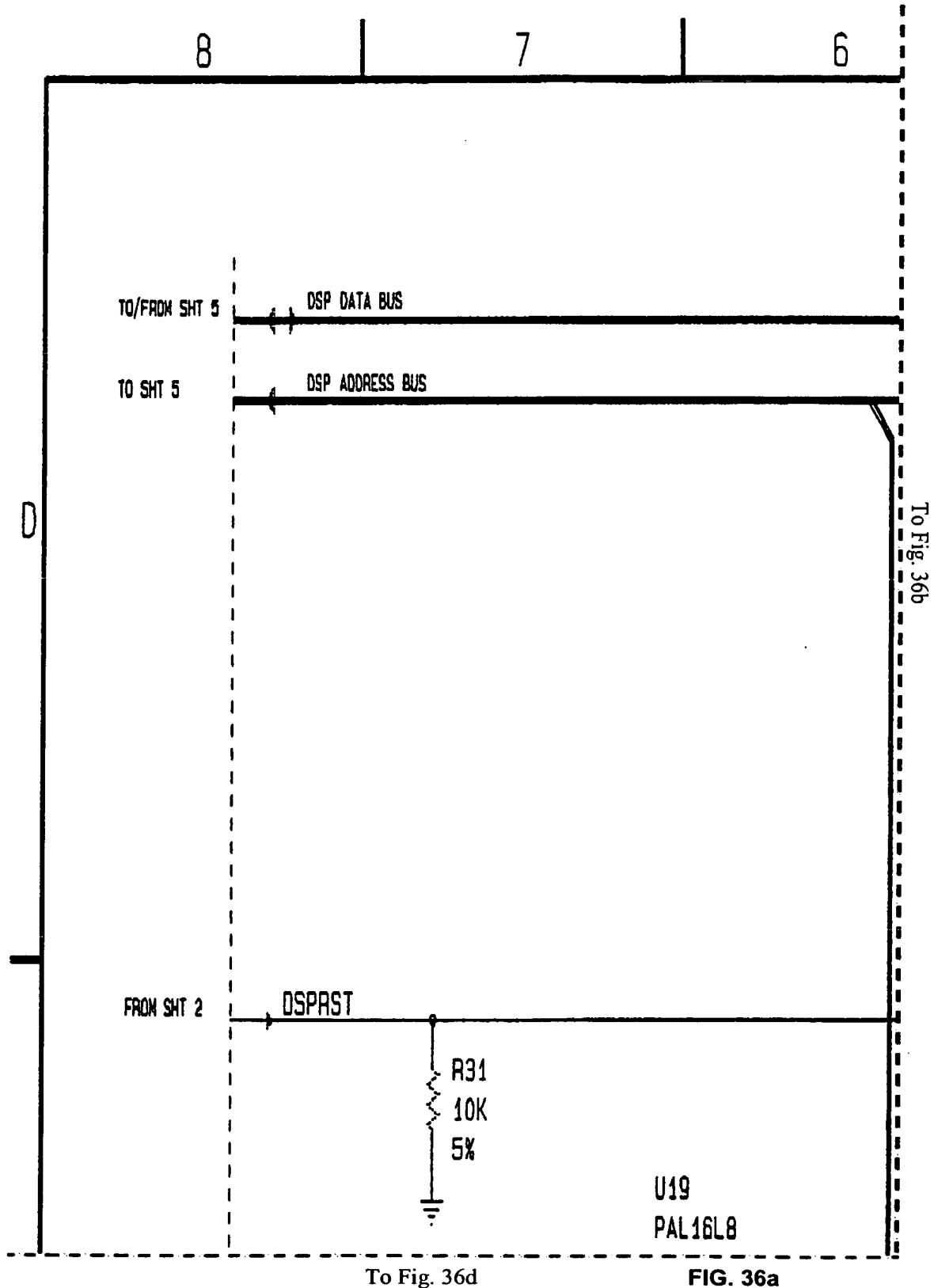
SHEET 5 OF 7

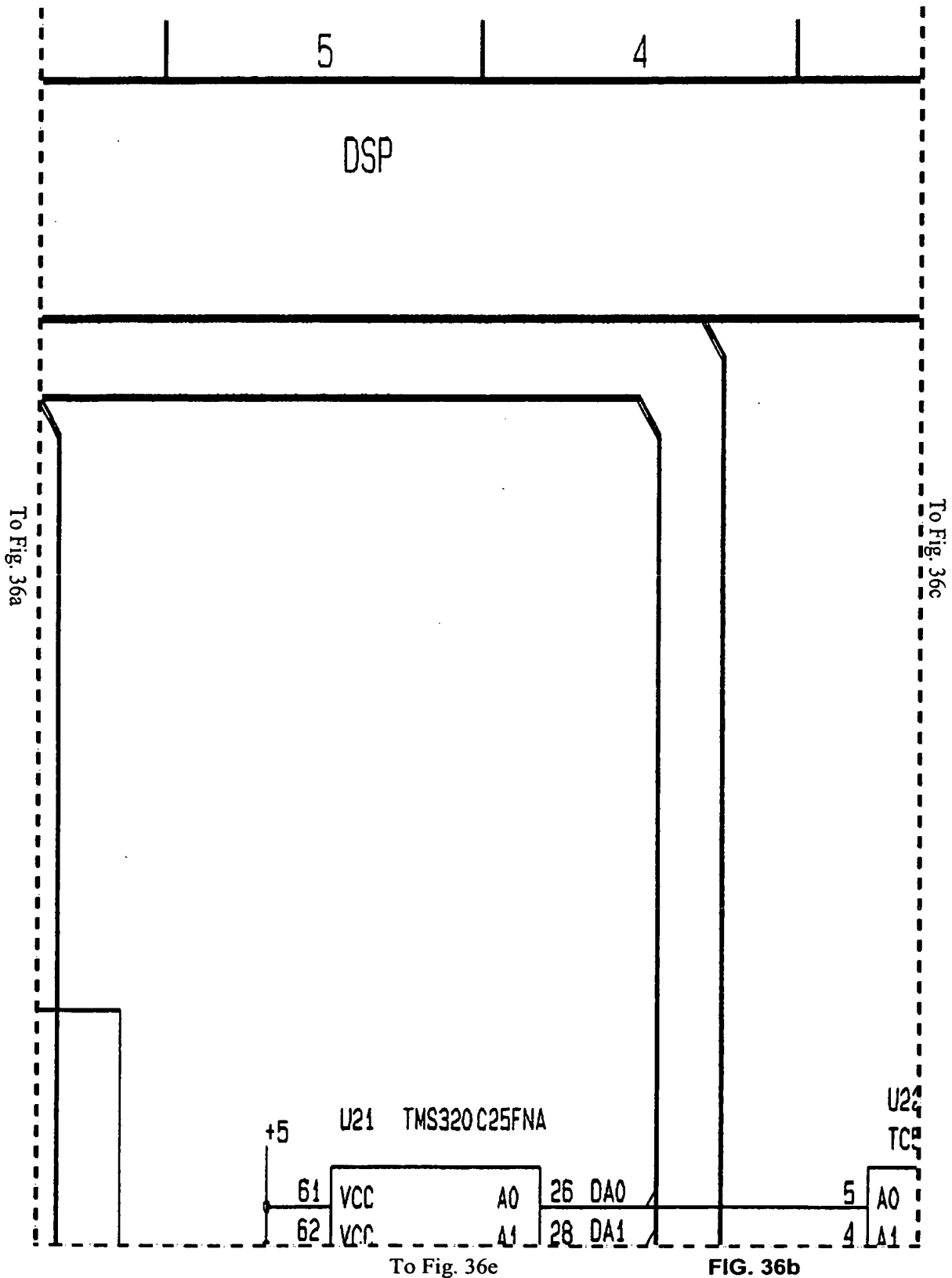
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FIG. 35i





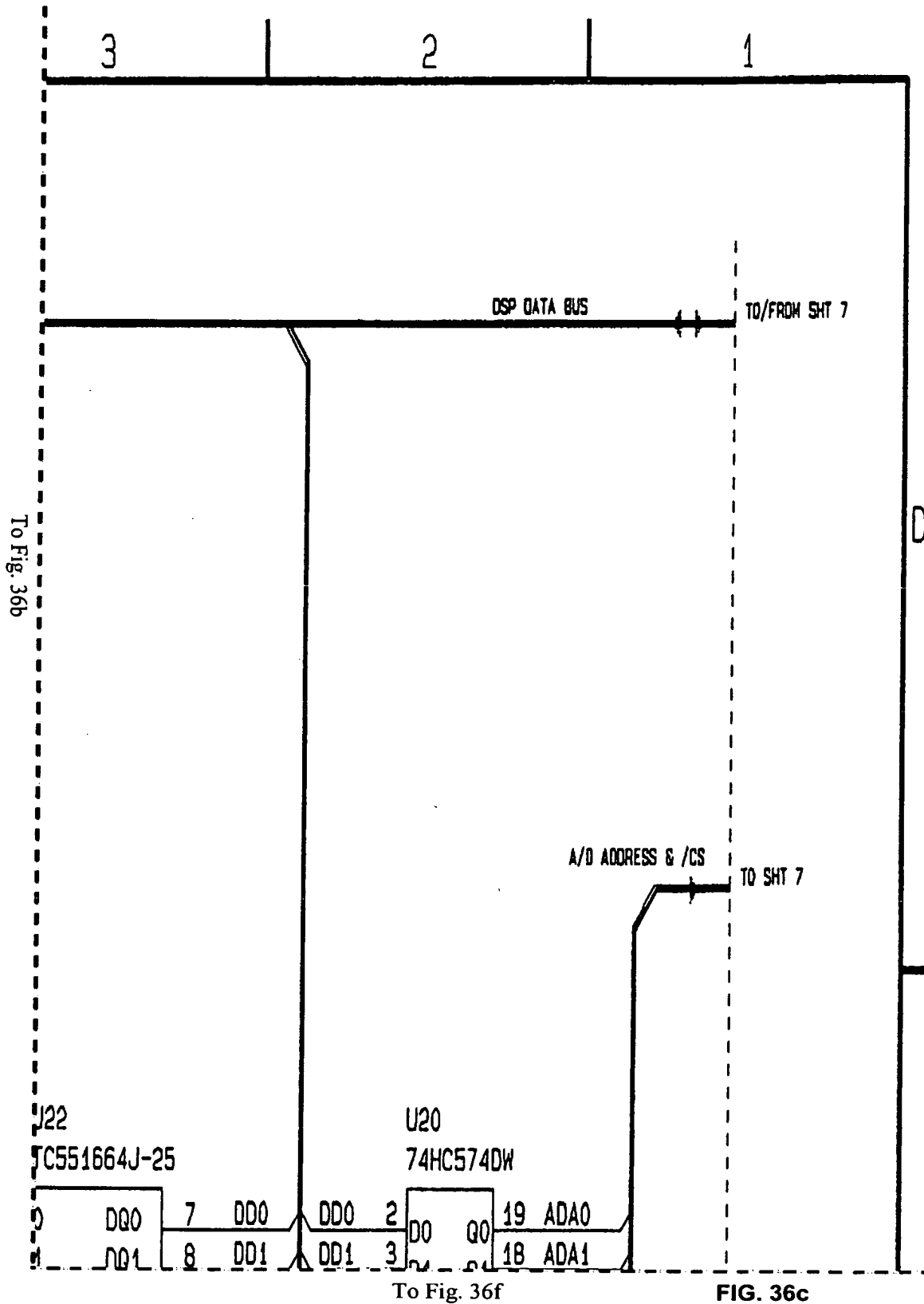
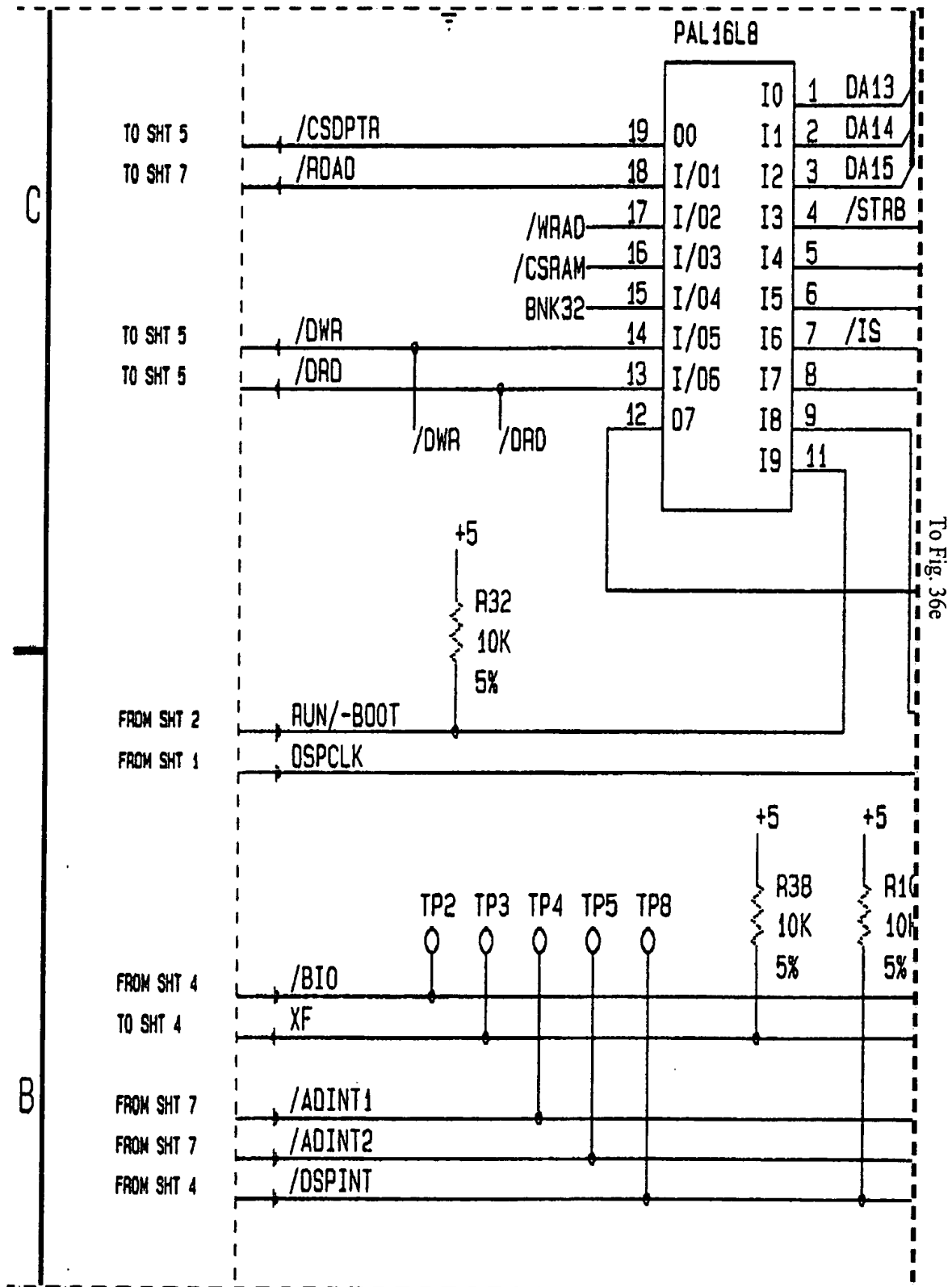


FIG. 36c



To Fig. 36a

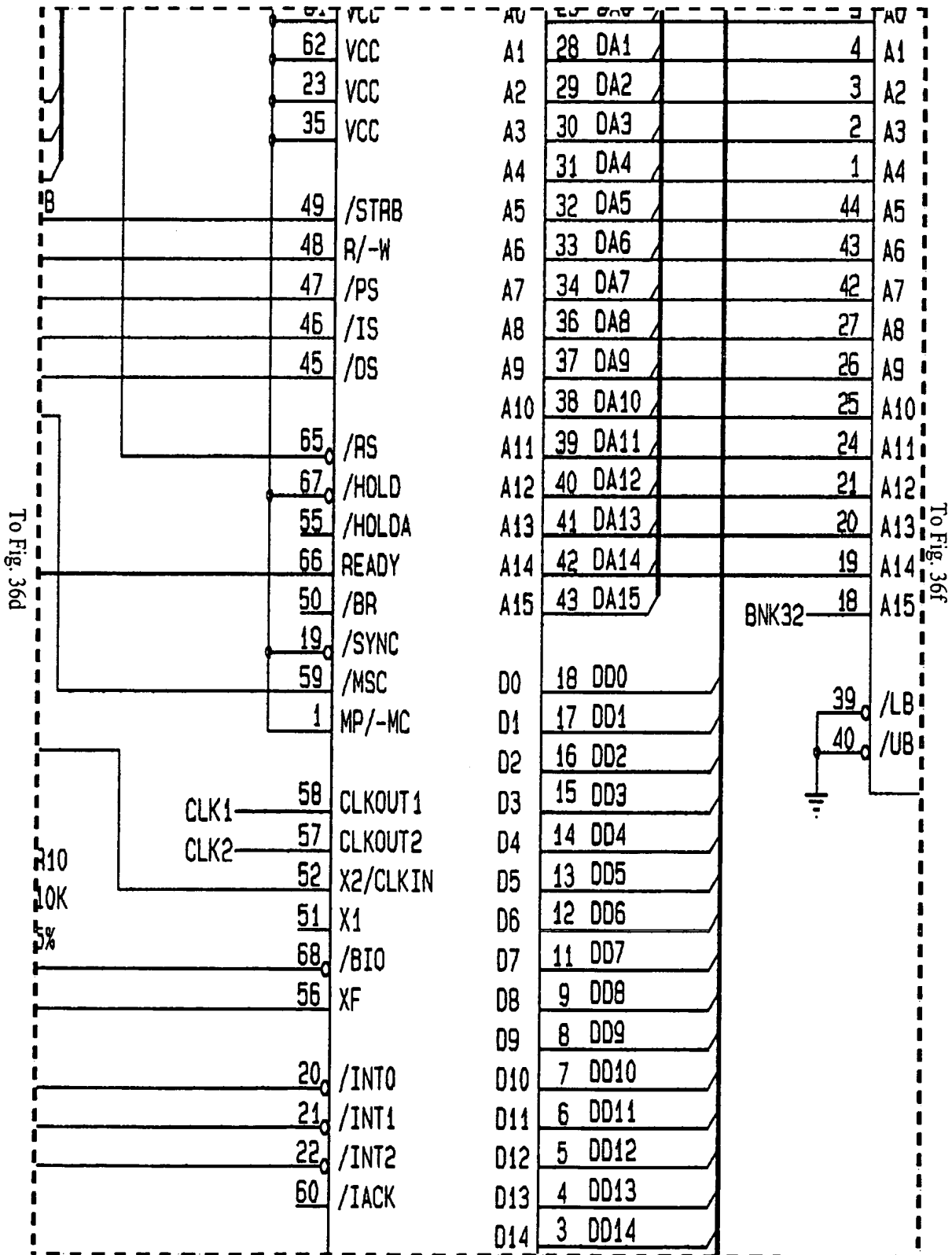


To Fig. 36e

To Fig. 36g

FIG. 36d

To Fig. 36b



To Fig. 36h

FIG. 36e

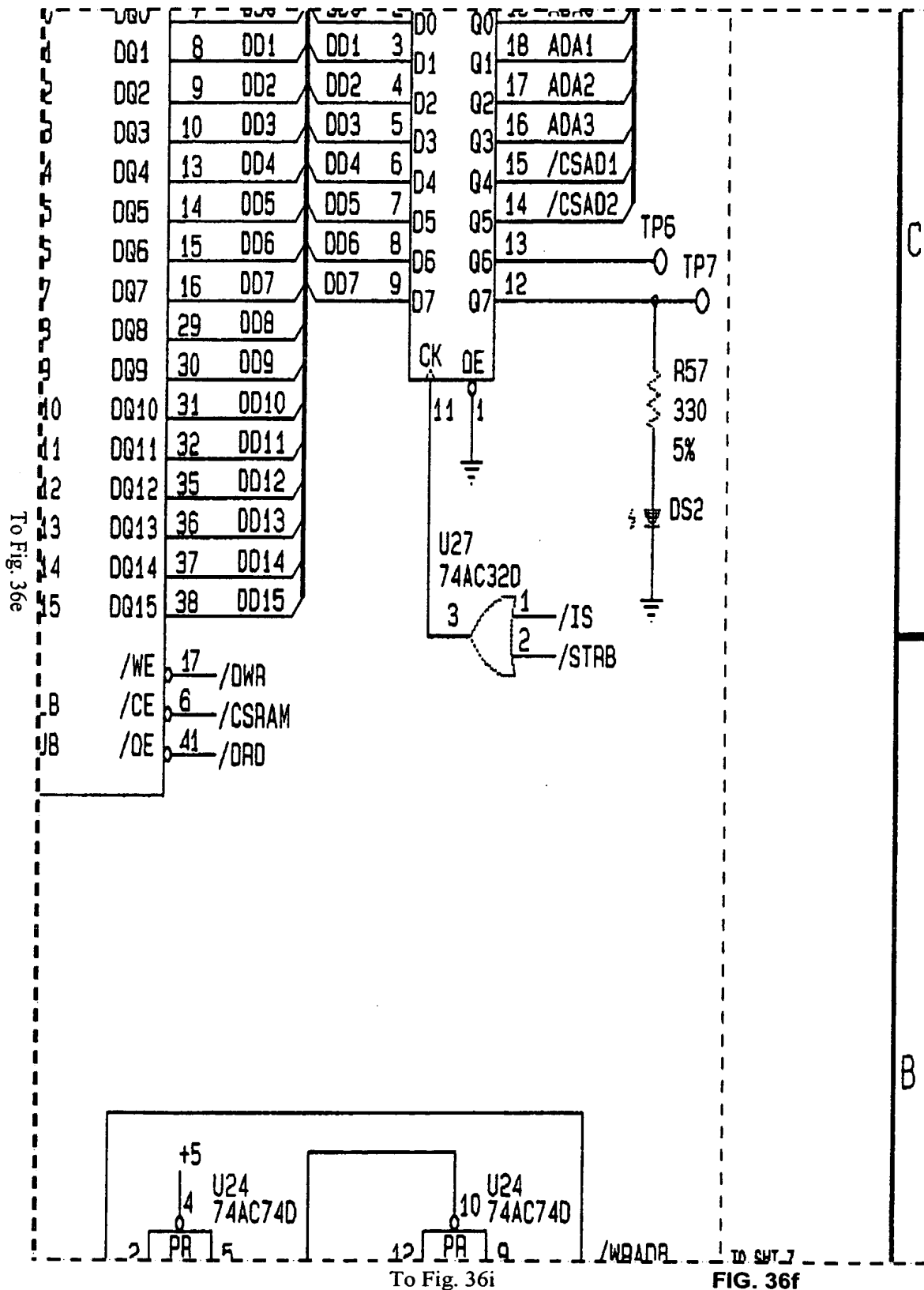
Patent Application For: PHASOR TRANSDUCER APPARATUS...

Inventor(s): Ronald G. Hart

Attorney Docket No.: 6270/109 - App. Ser. #10/613,611

New Sheet

To Fig. 36c



To Fig. 36d

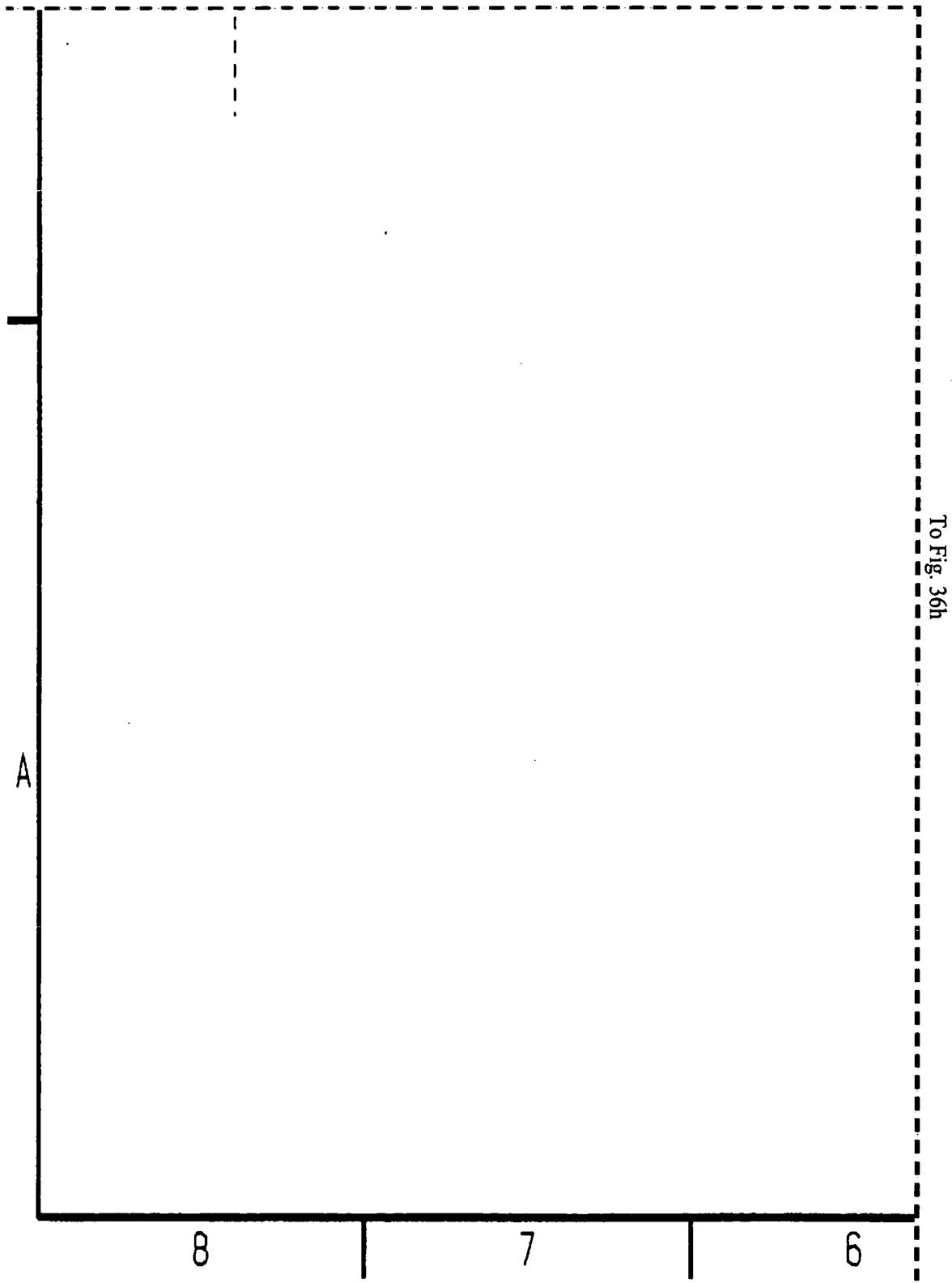


FIG. 36g

To Fig. 36e

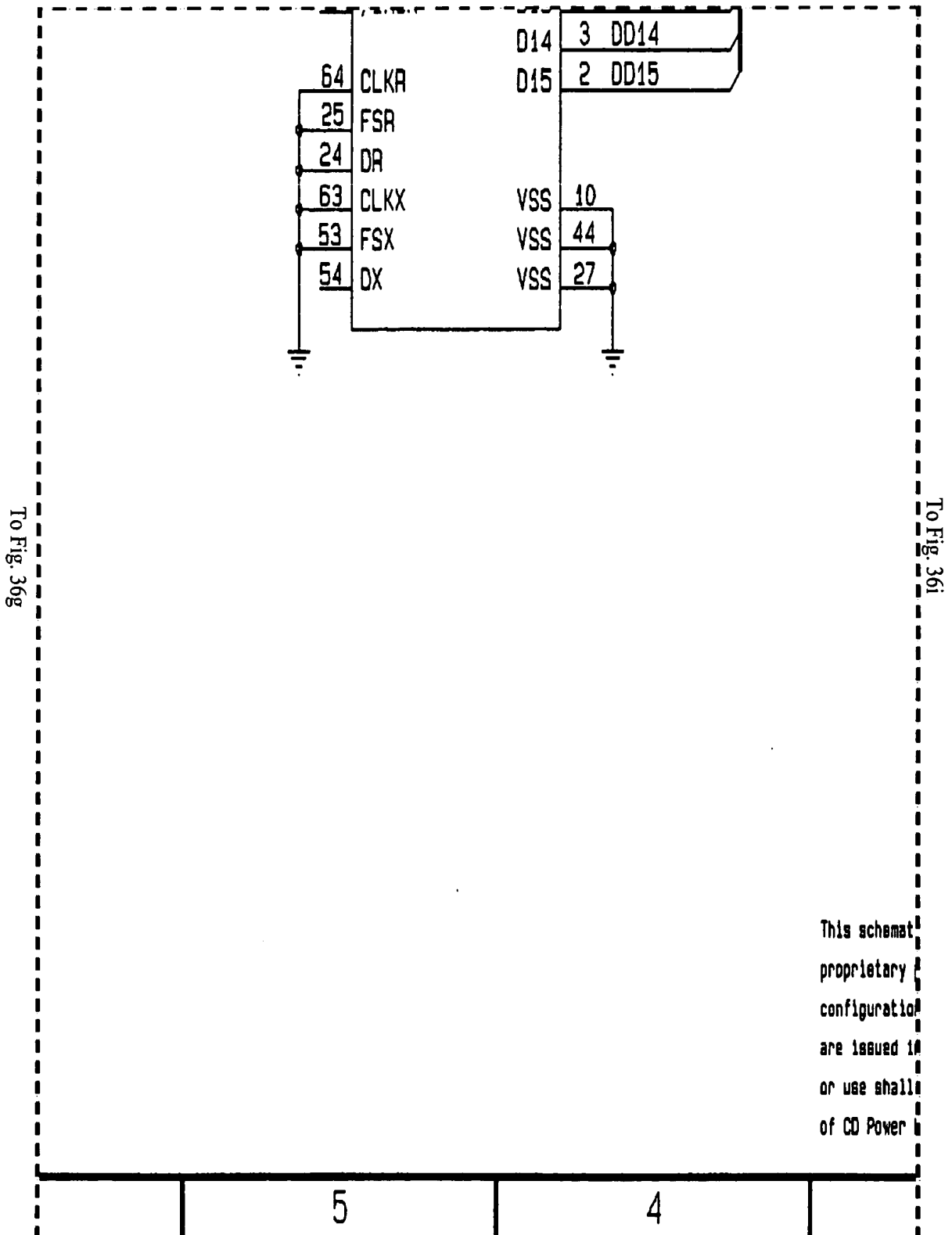
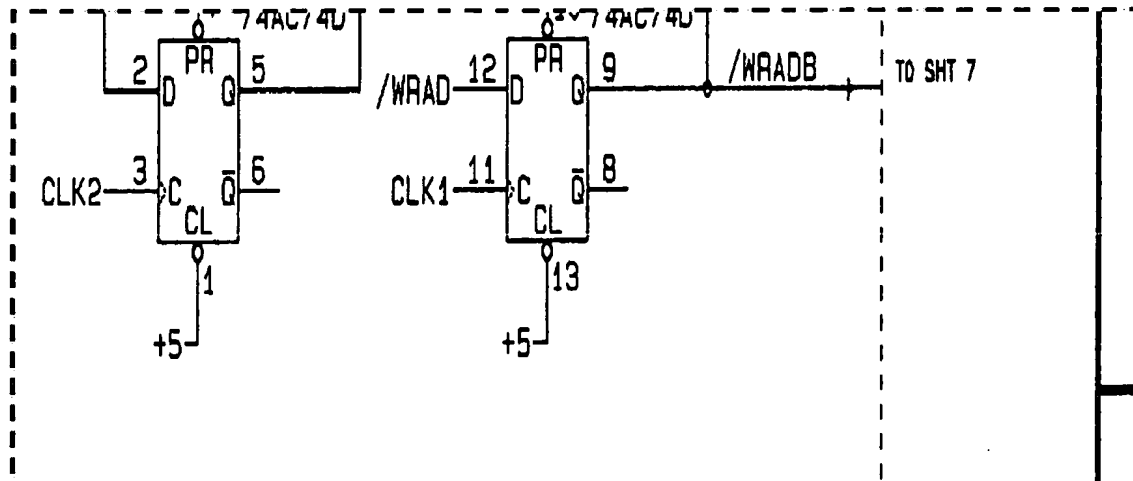


FIG. 36h

To Fig. 36f



To Fig. 36h

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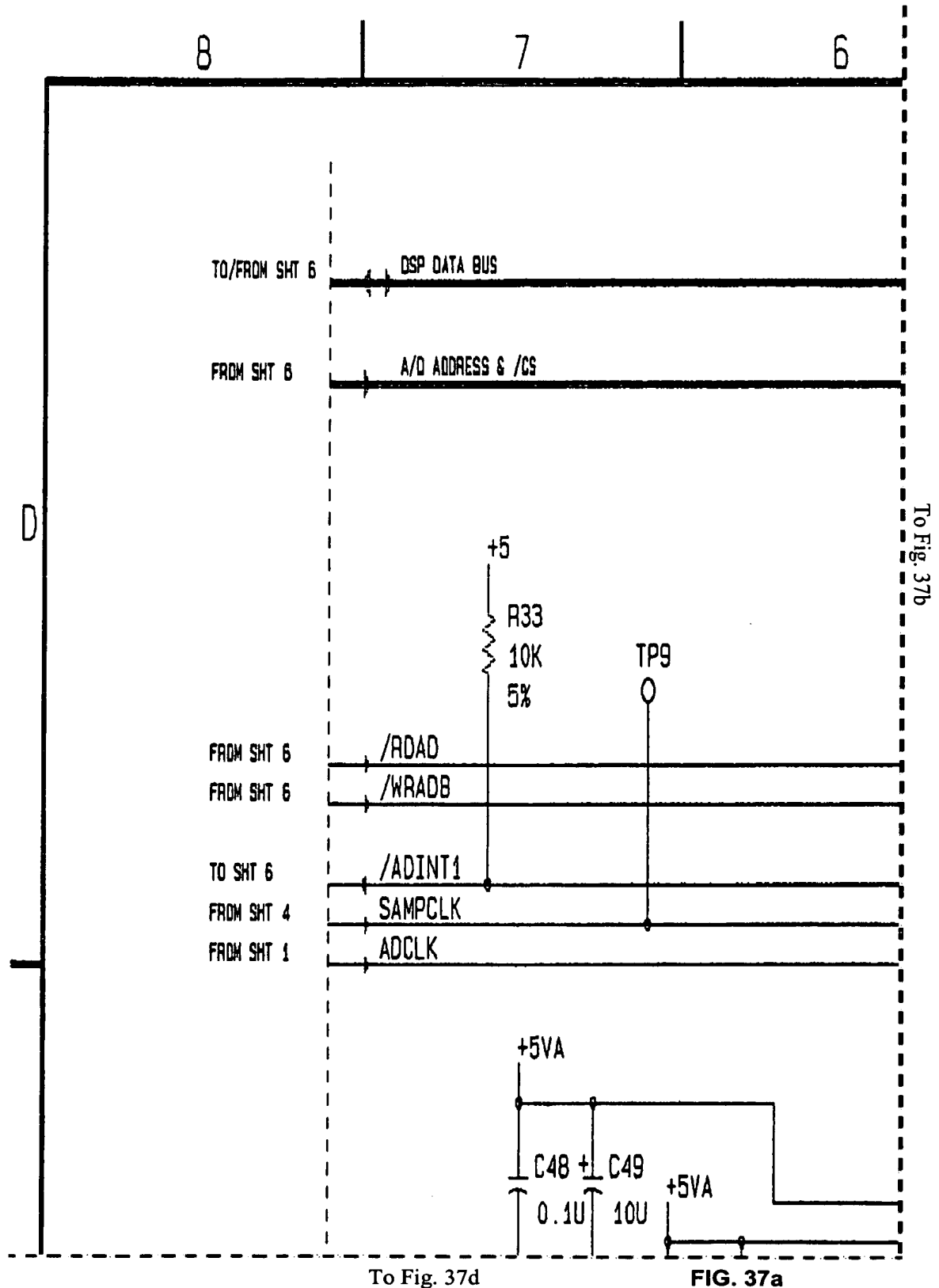
SHEET 6 OF 7

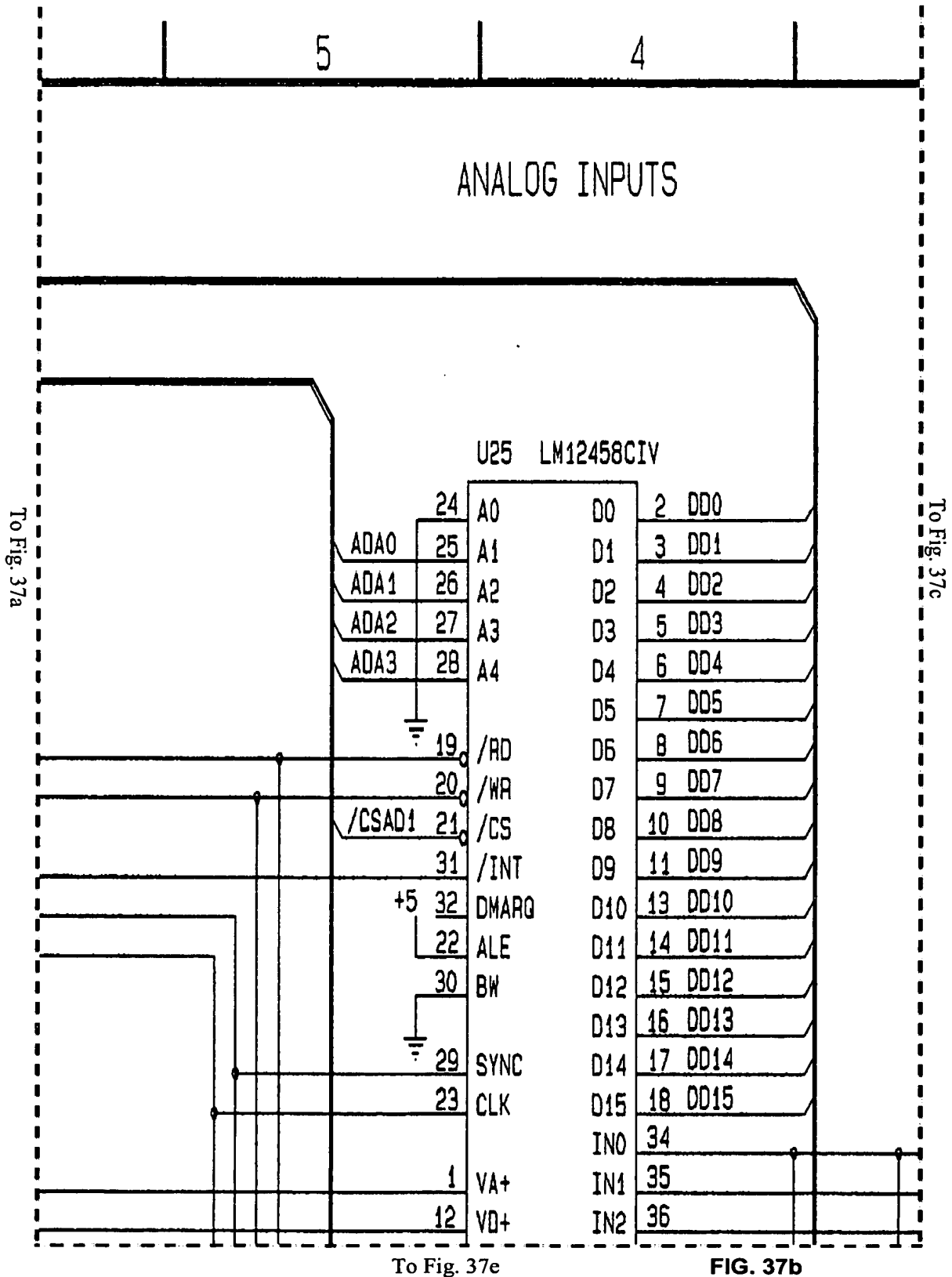
3

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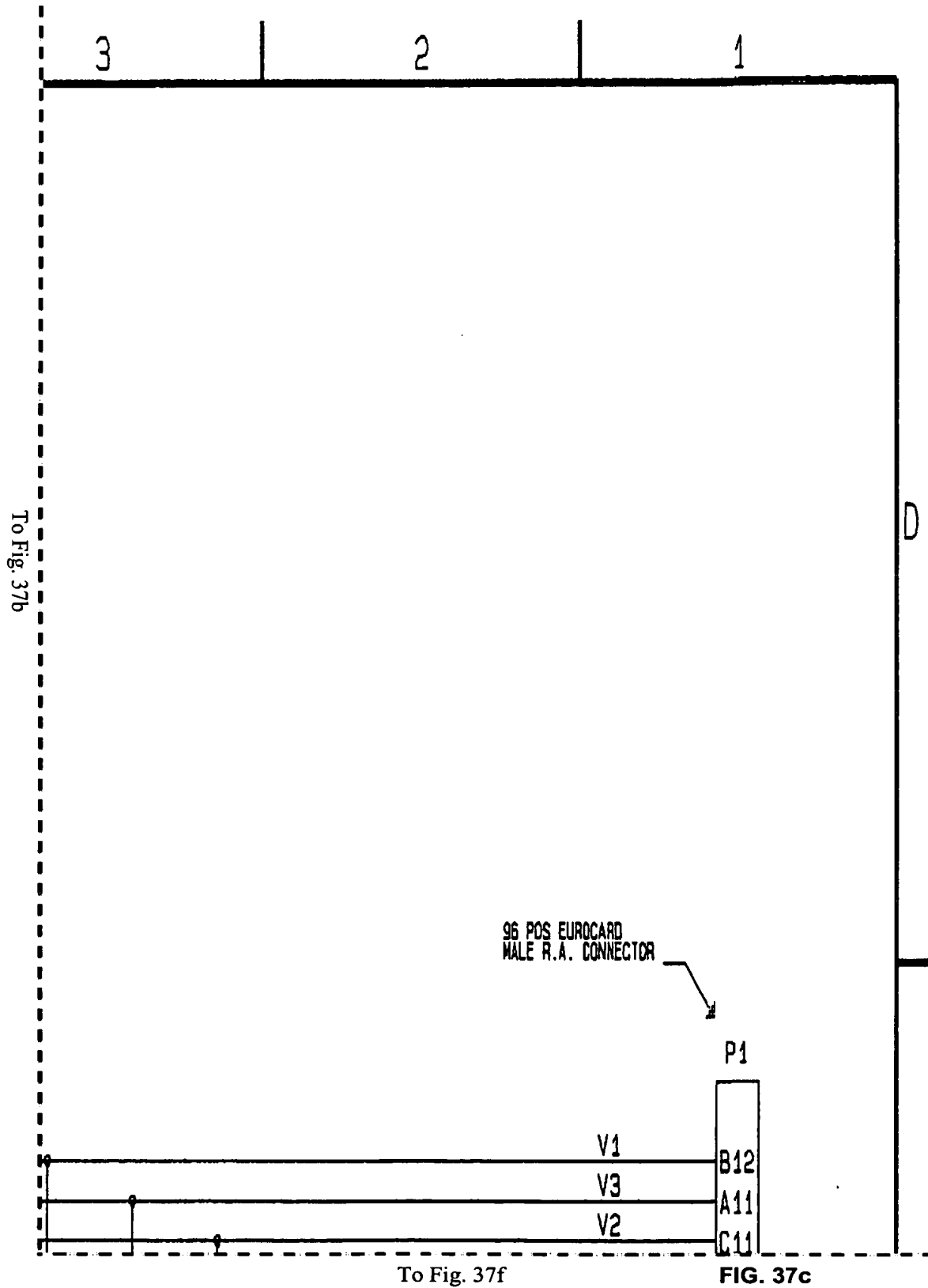
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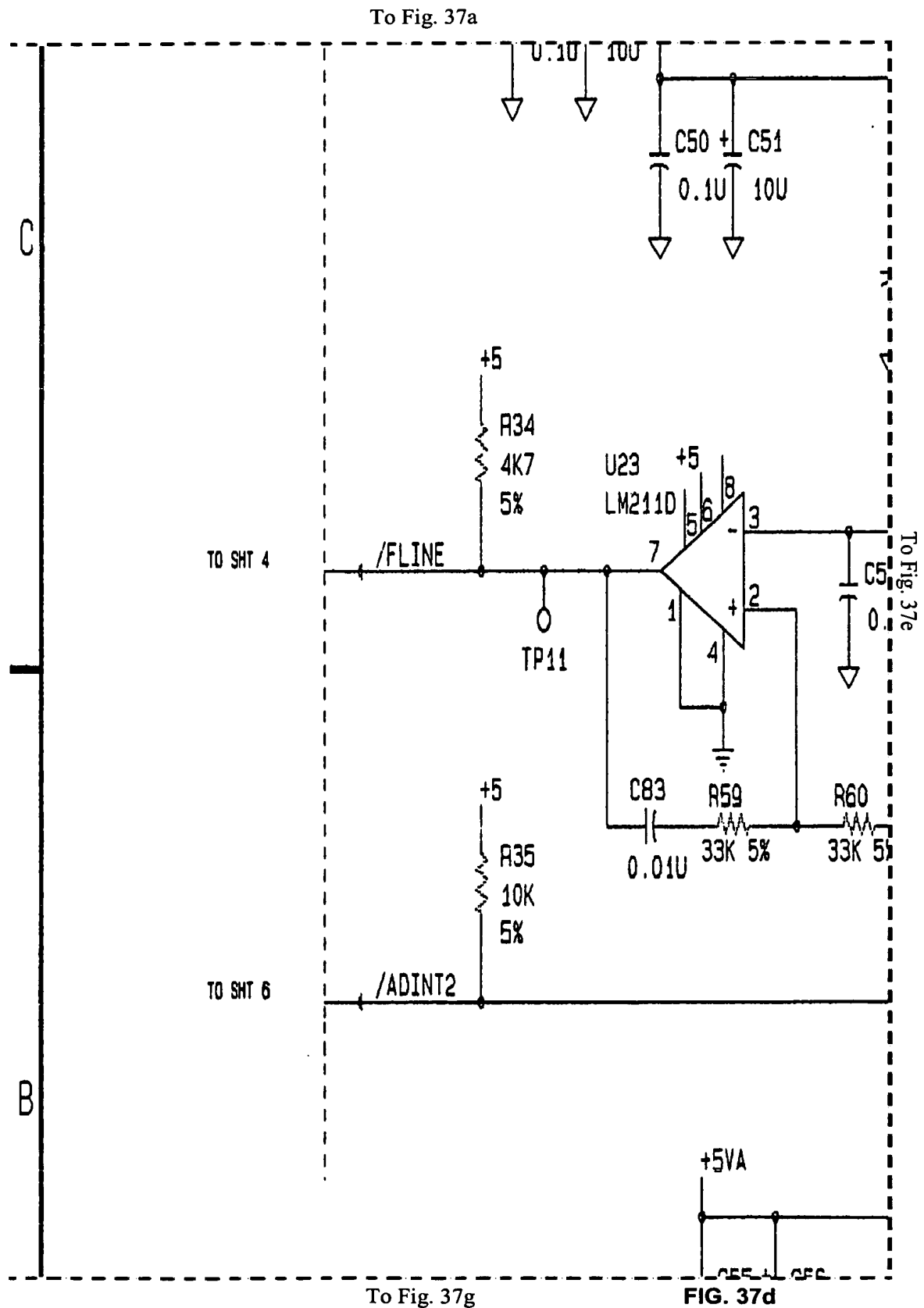
FIG. 36i



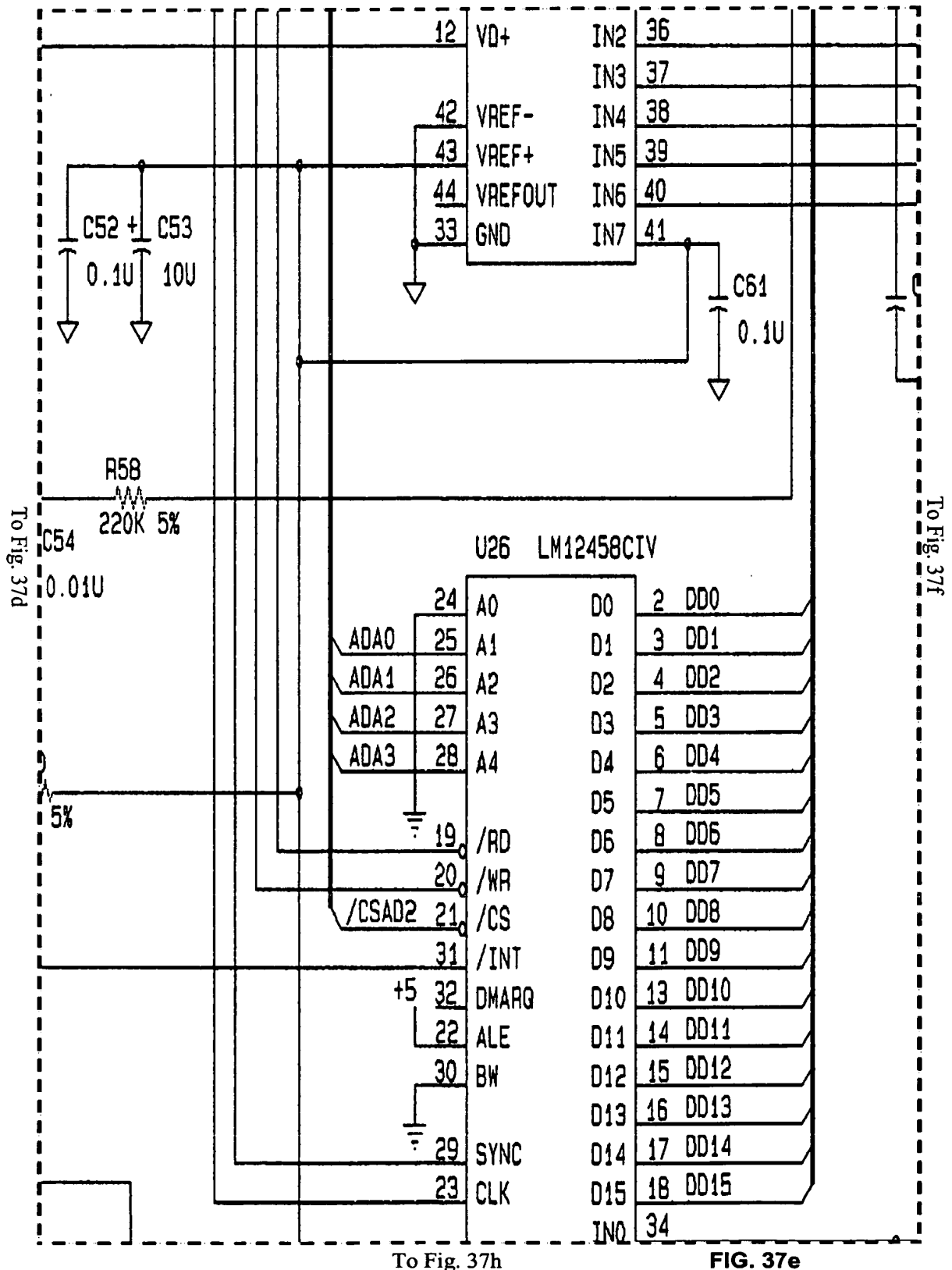




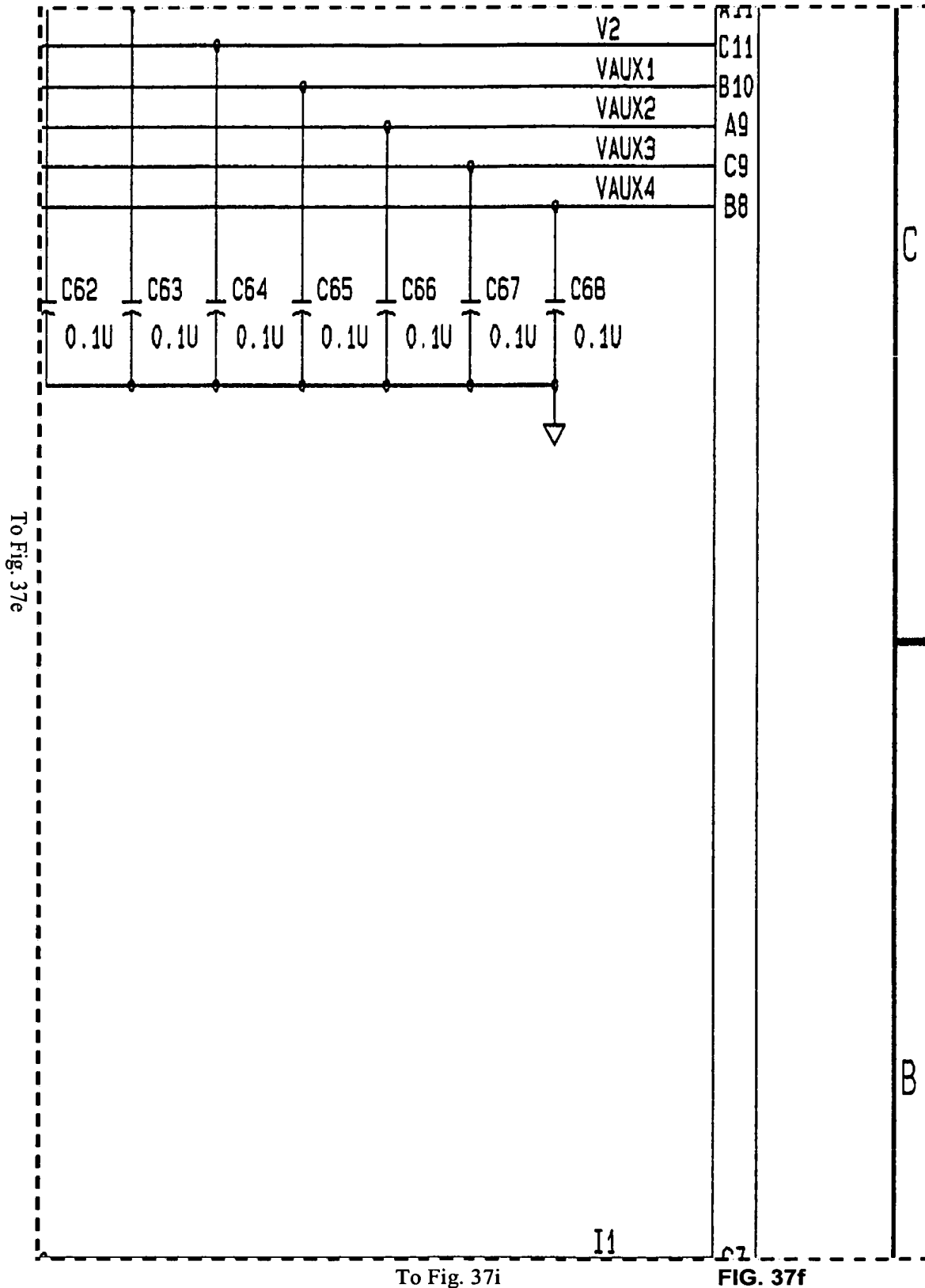




To Fig. 37b



To Fig. 37c



To Fig. 37d

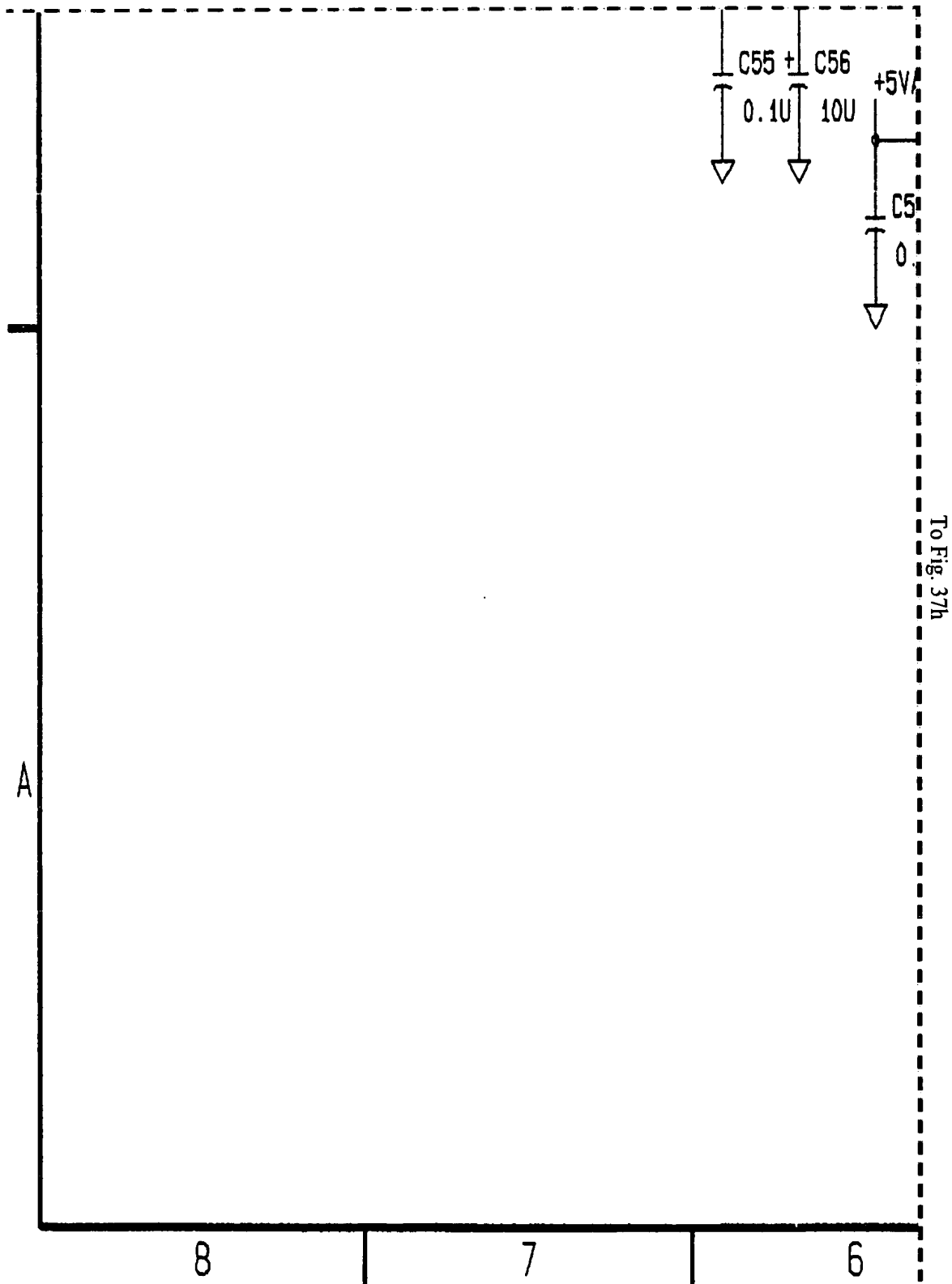
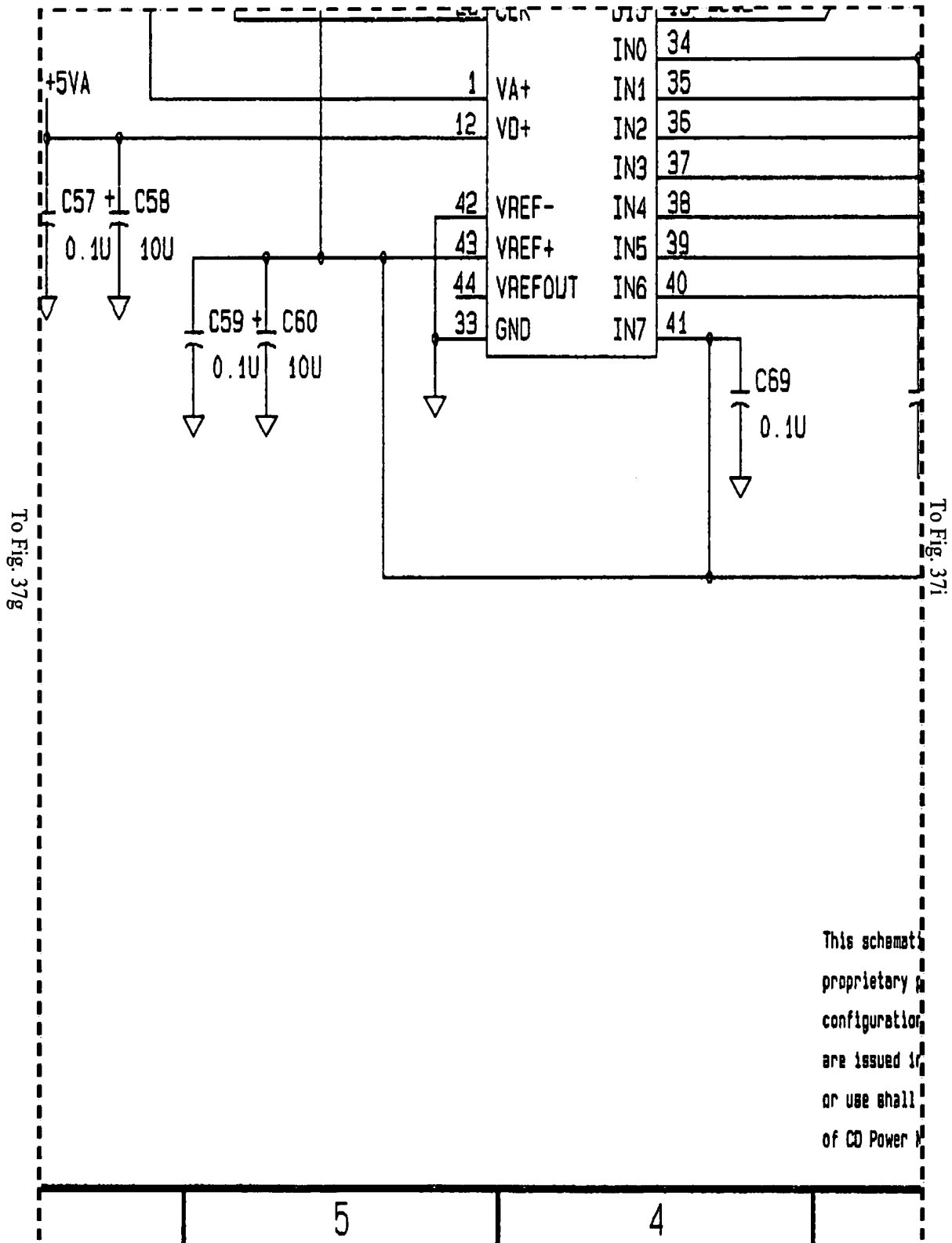


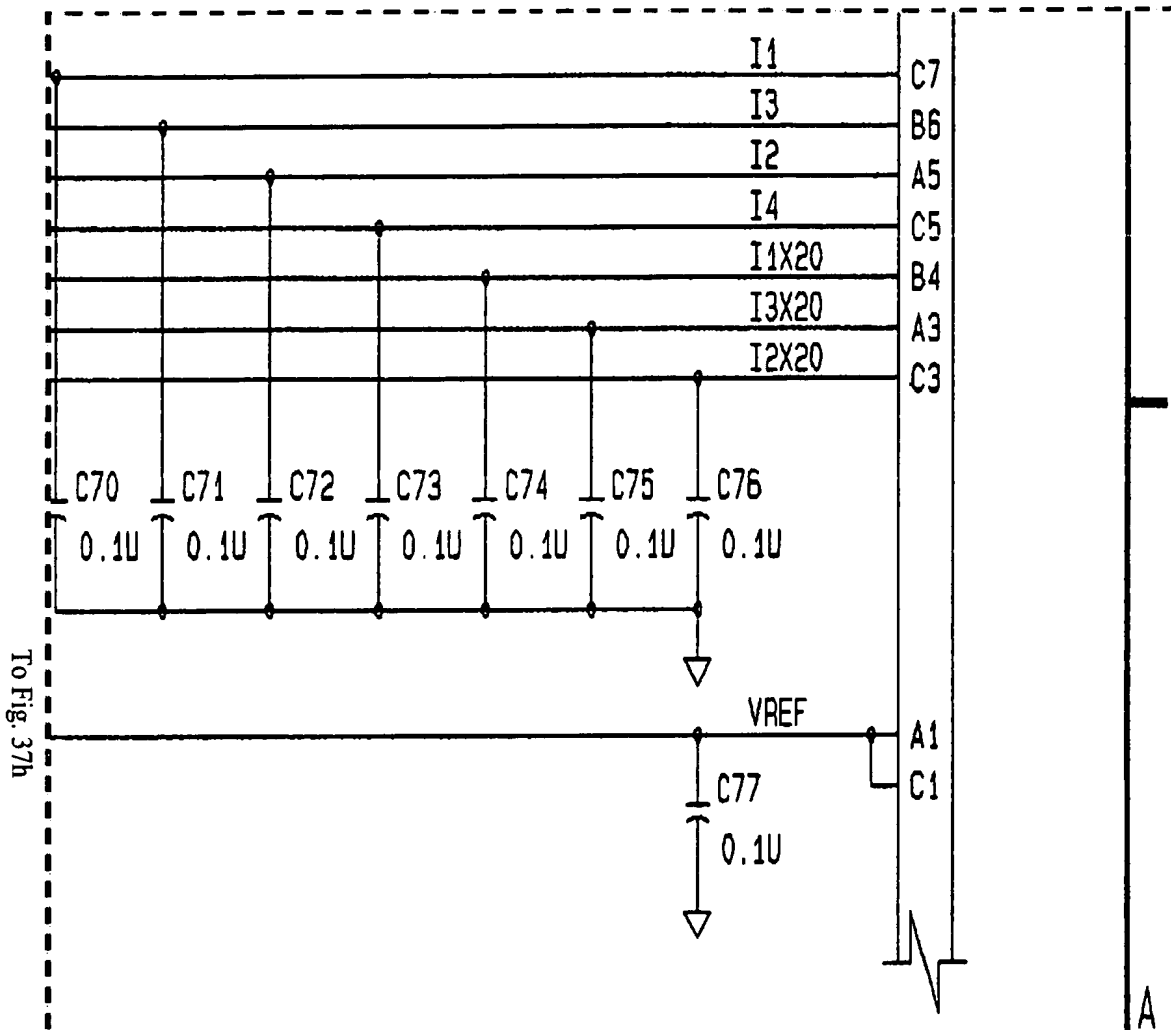
FIG. 37g

To Fig. 37e



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To Fig. 37f



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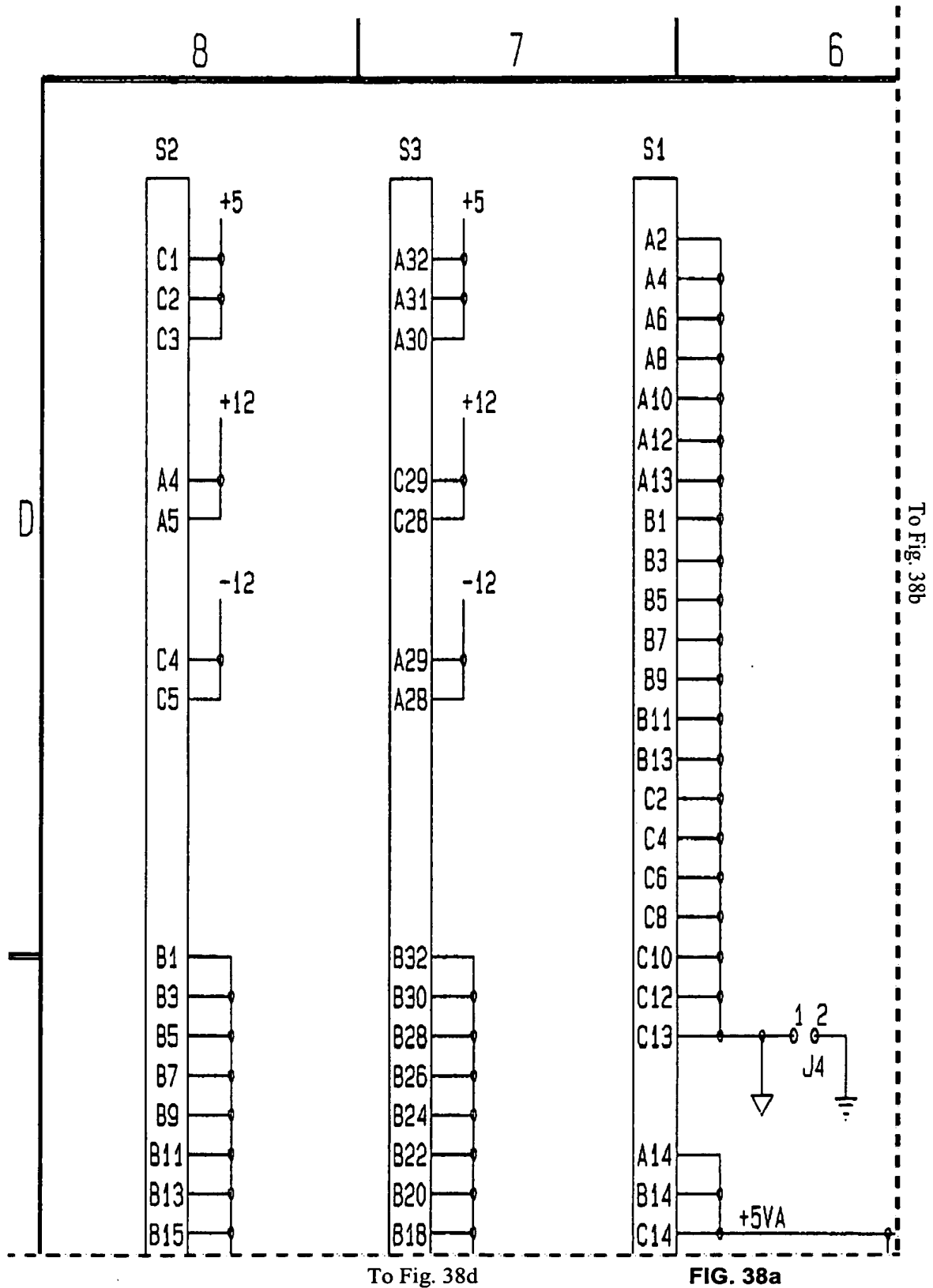
SHEET 7 OF 7

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1

FIG. 37i





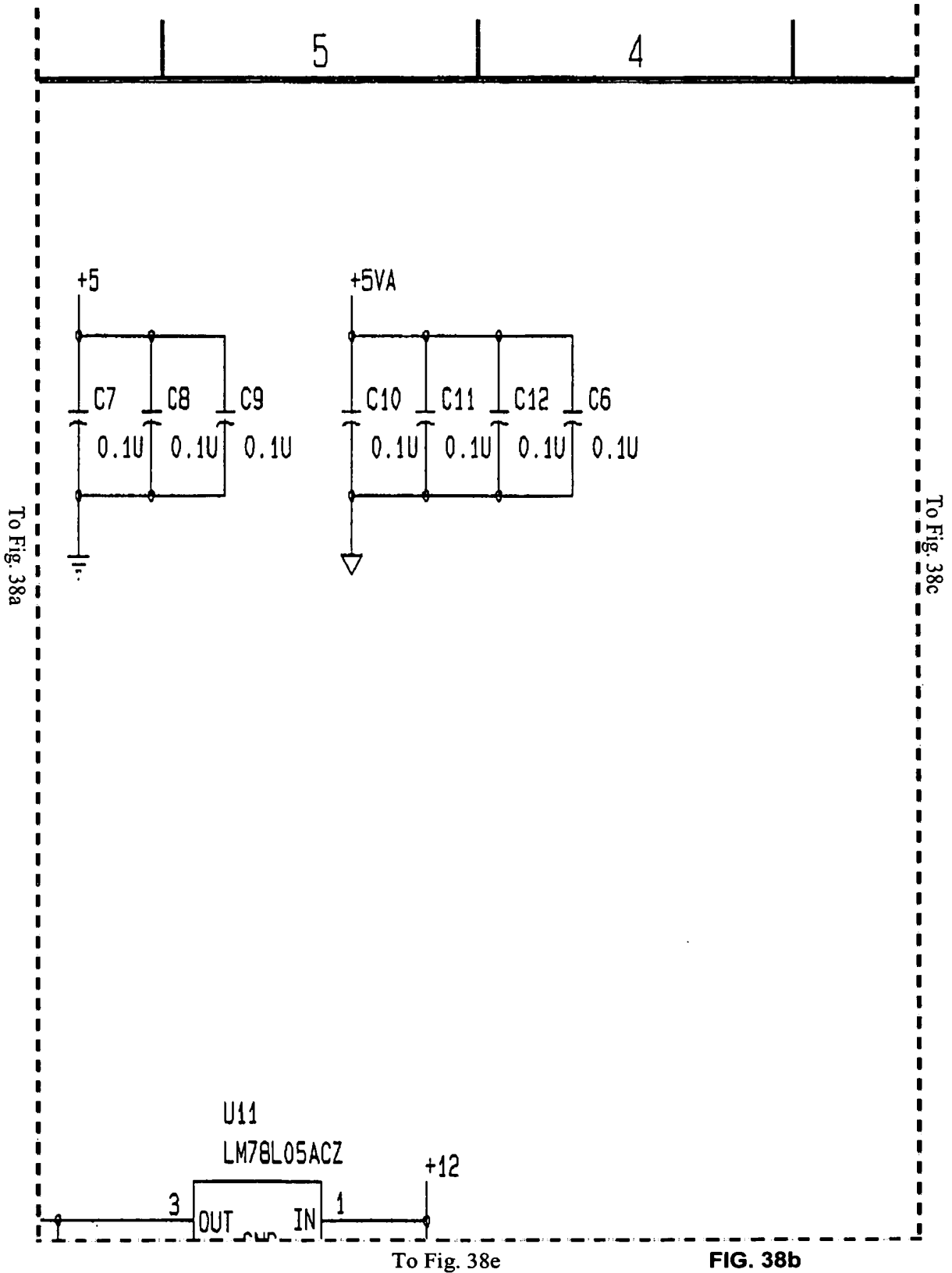
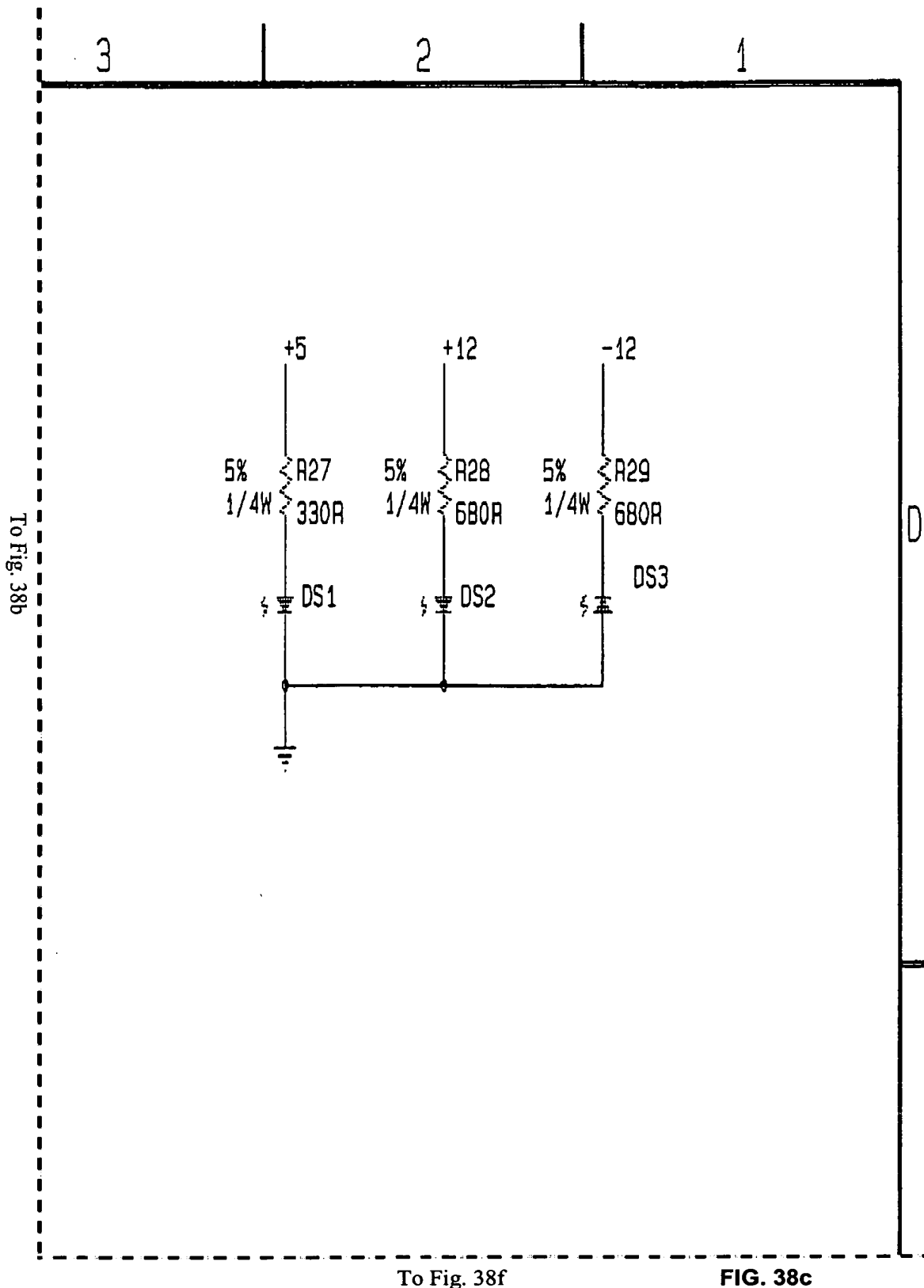
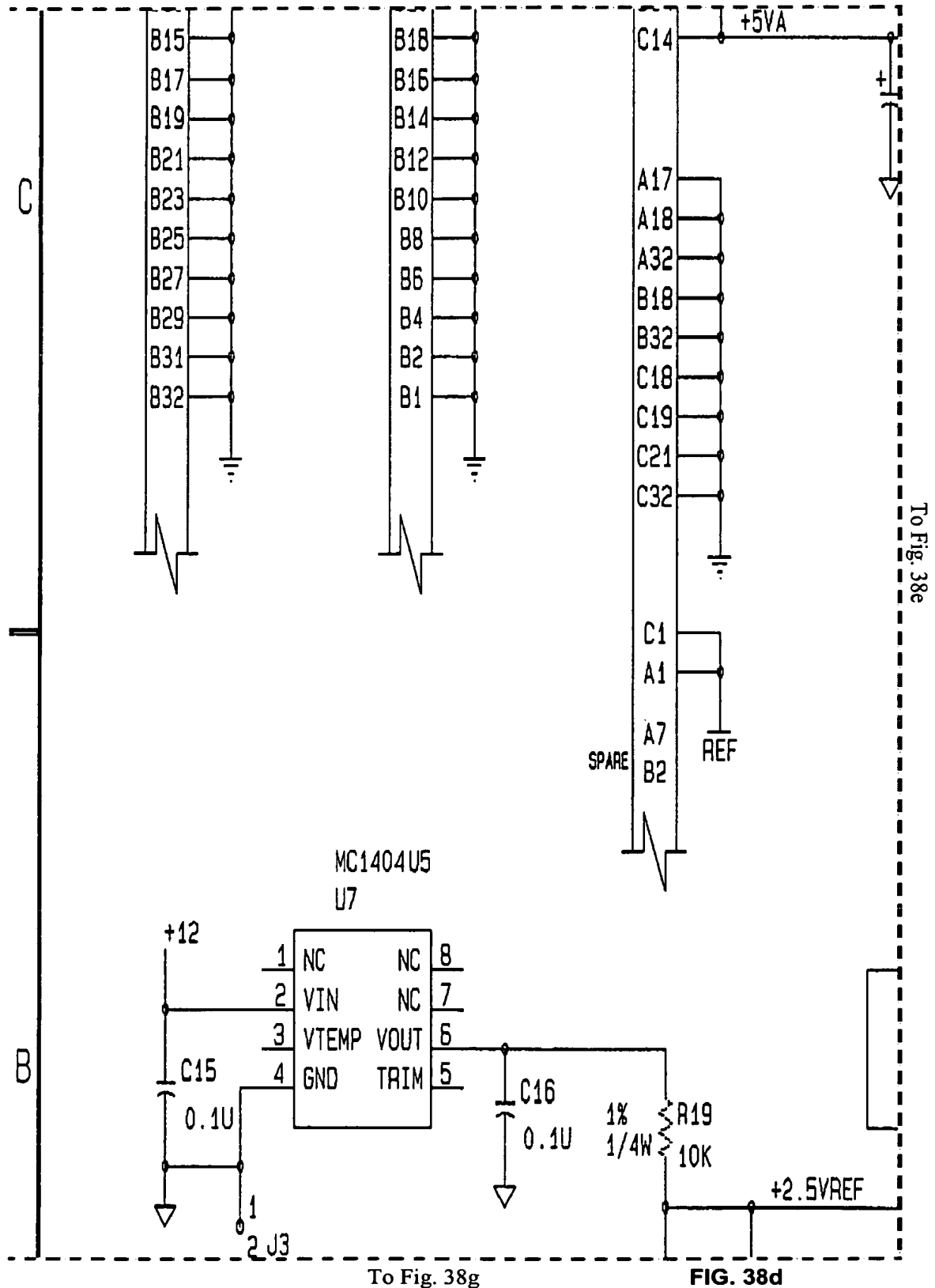


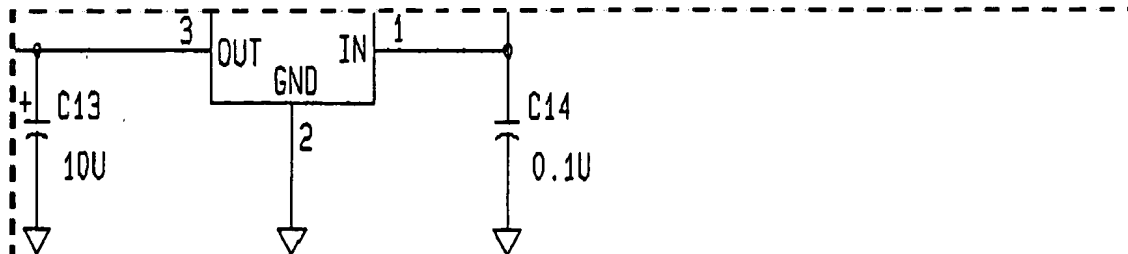
FIG. 38b



To Fig. 38a

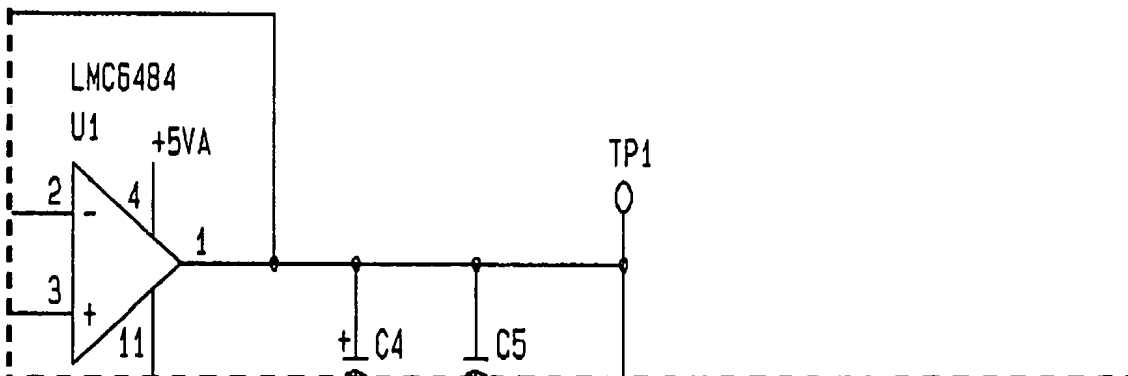


To Fig. 38b



To Fig. 38d

To Fig. 38f



To Fig. 38h

FIG. 38e

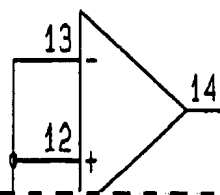
To Fig. 38c

To Fig. 38e

SPARES

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U10



To Fig. 38i

FIG. 38f

C

B

To Fig. 38d

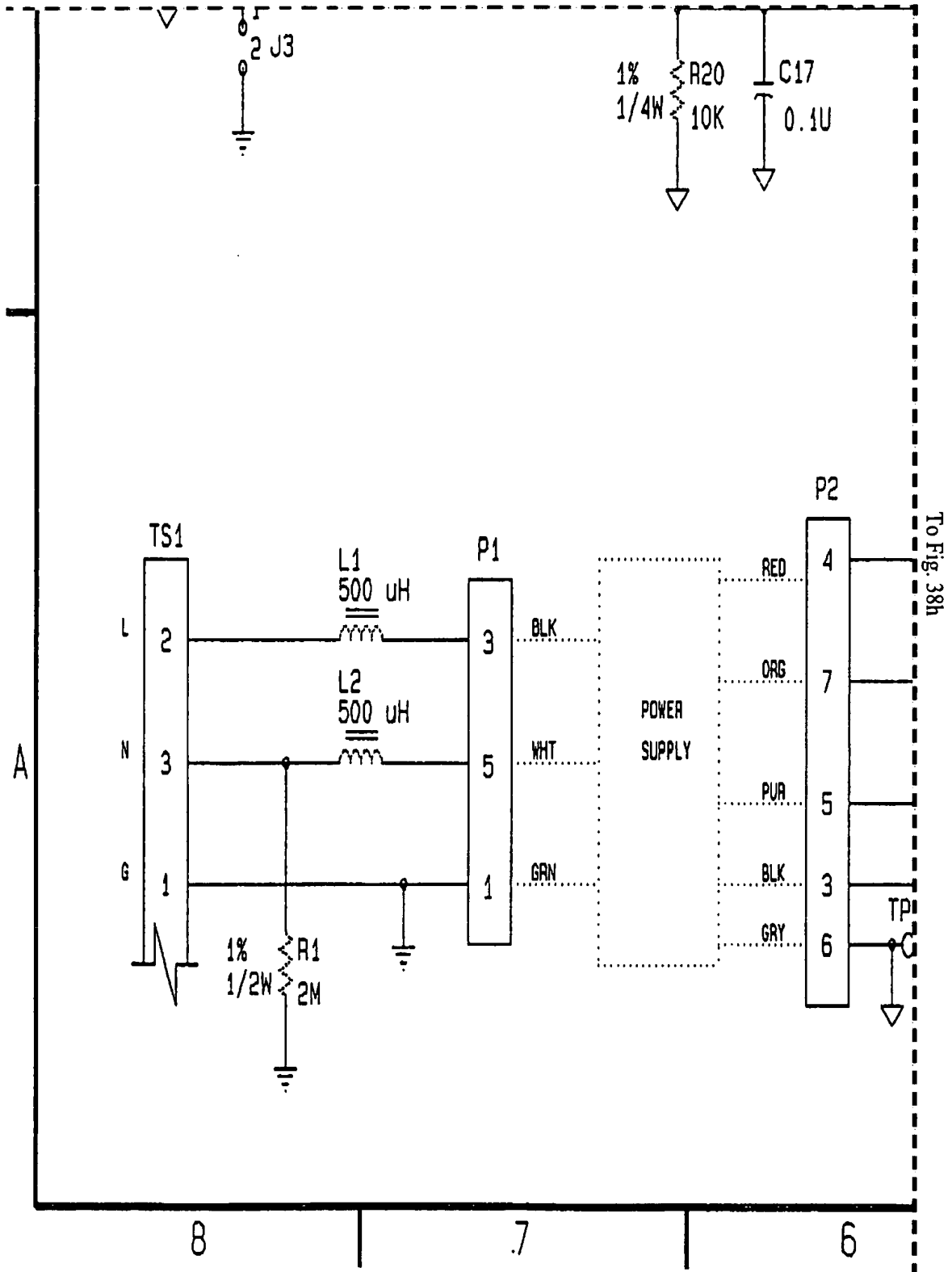
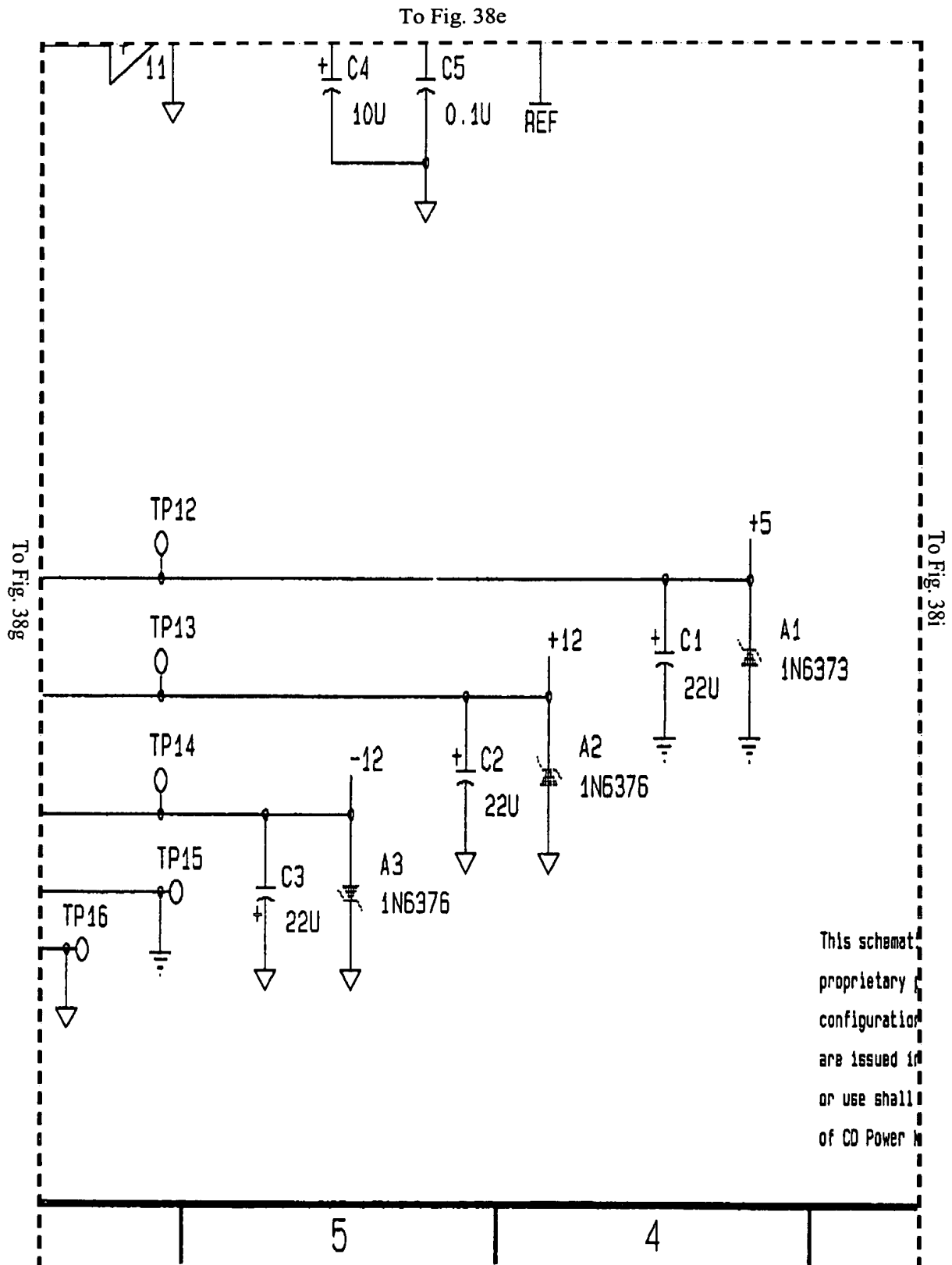


FIG. 38g



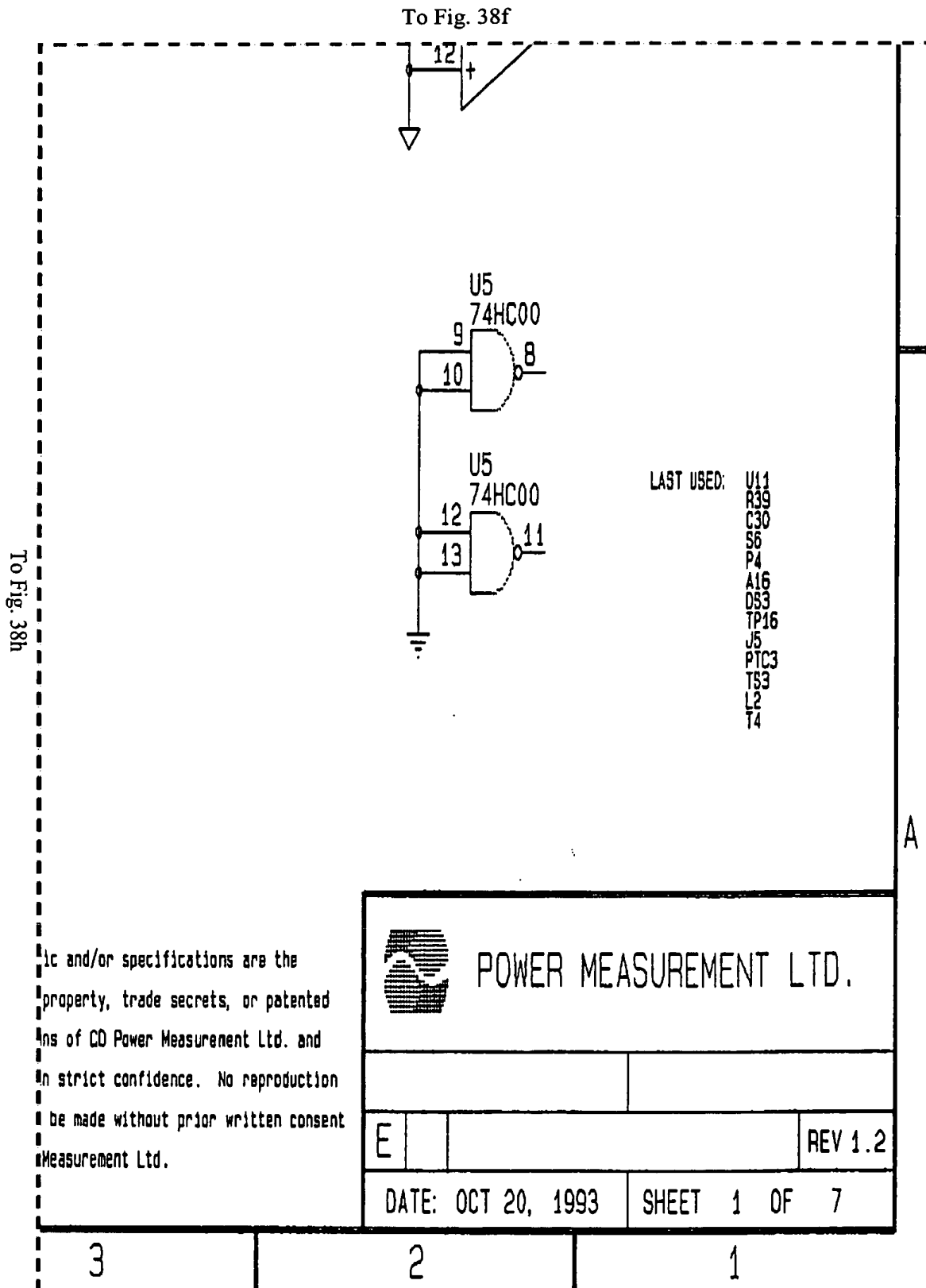
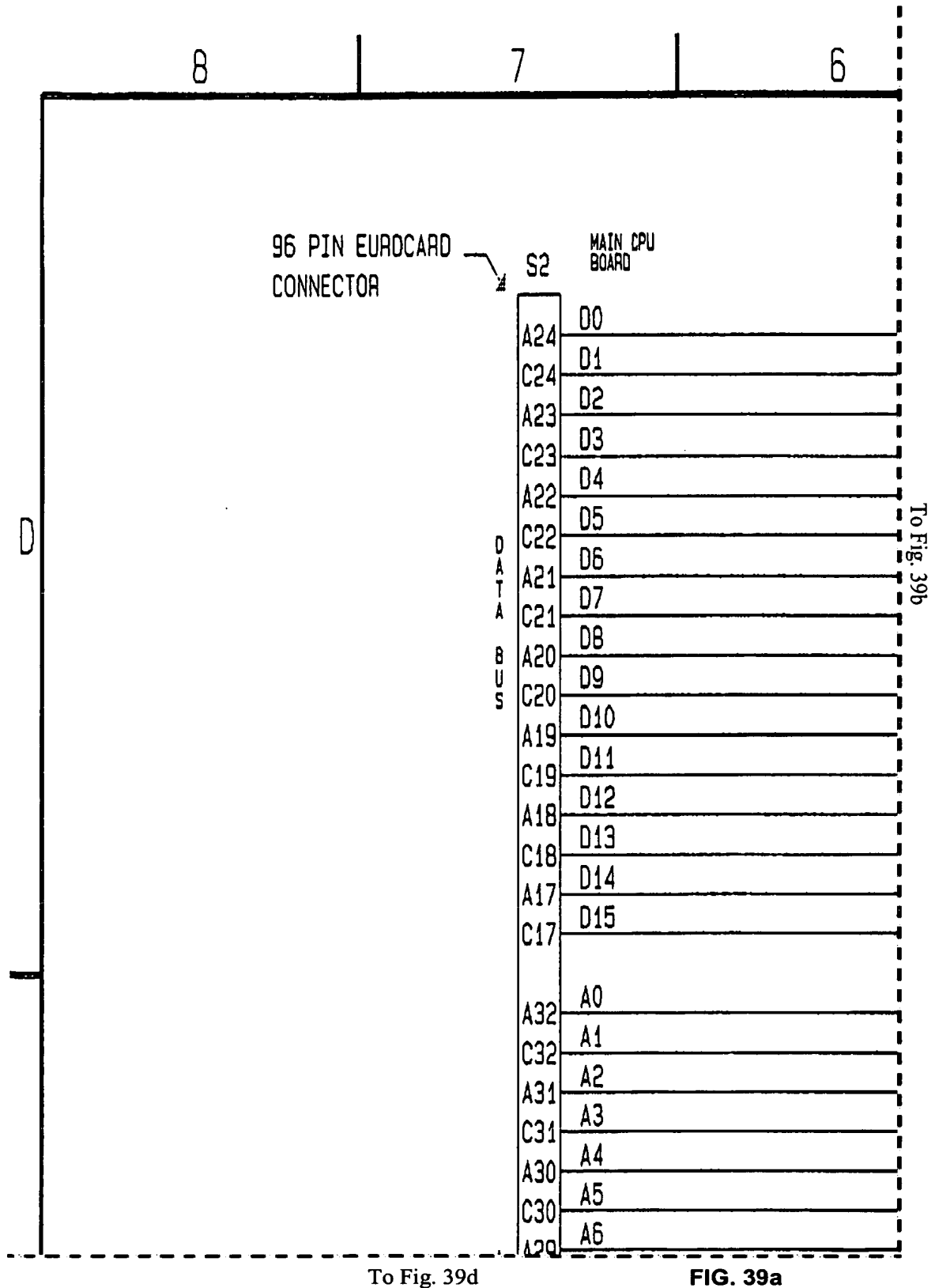
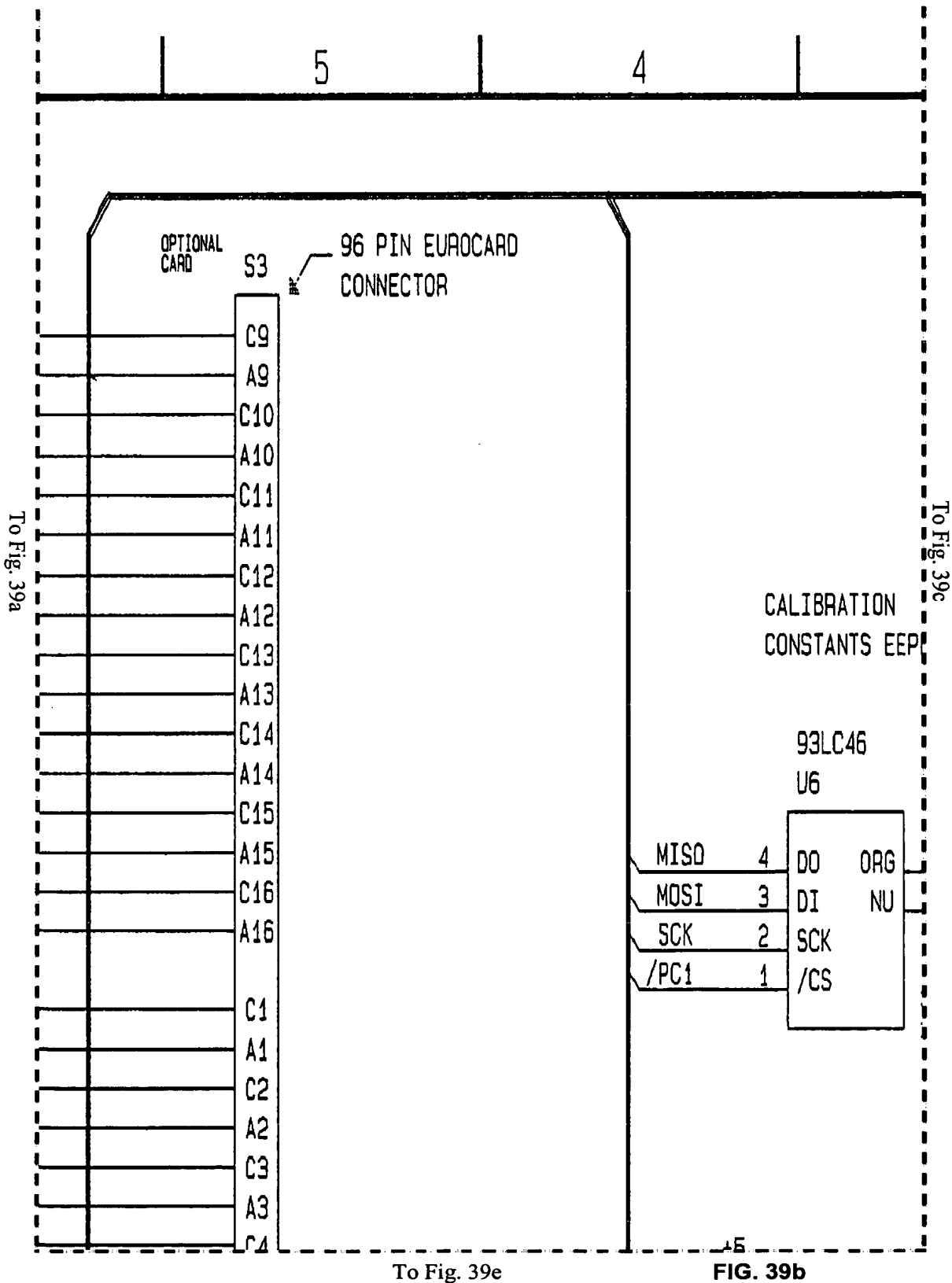
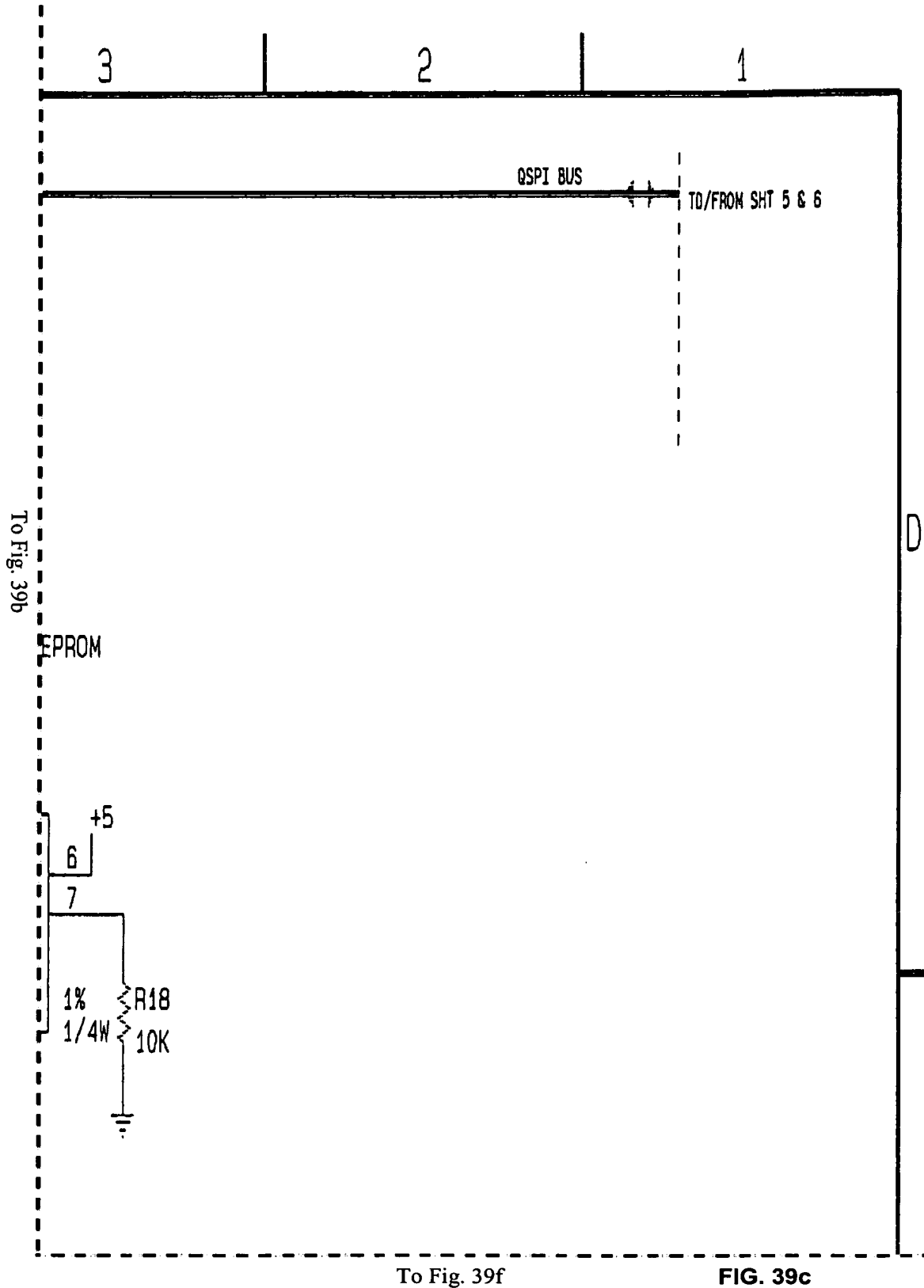


FIG. 38i

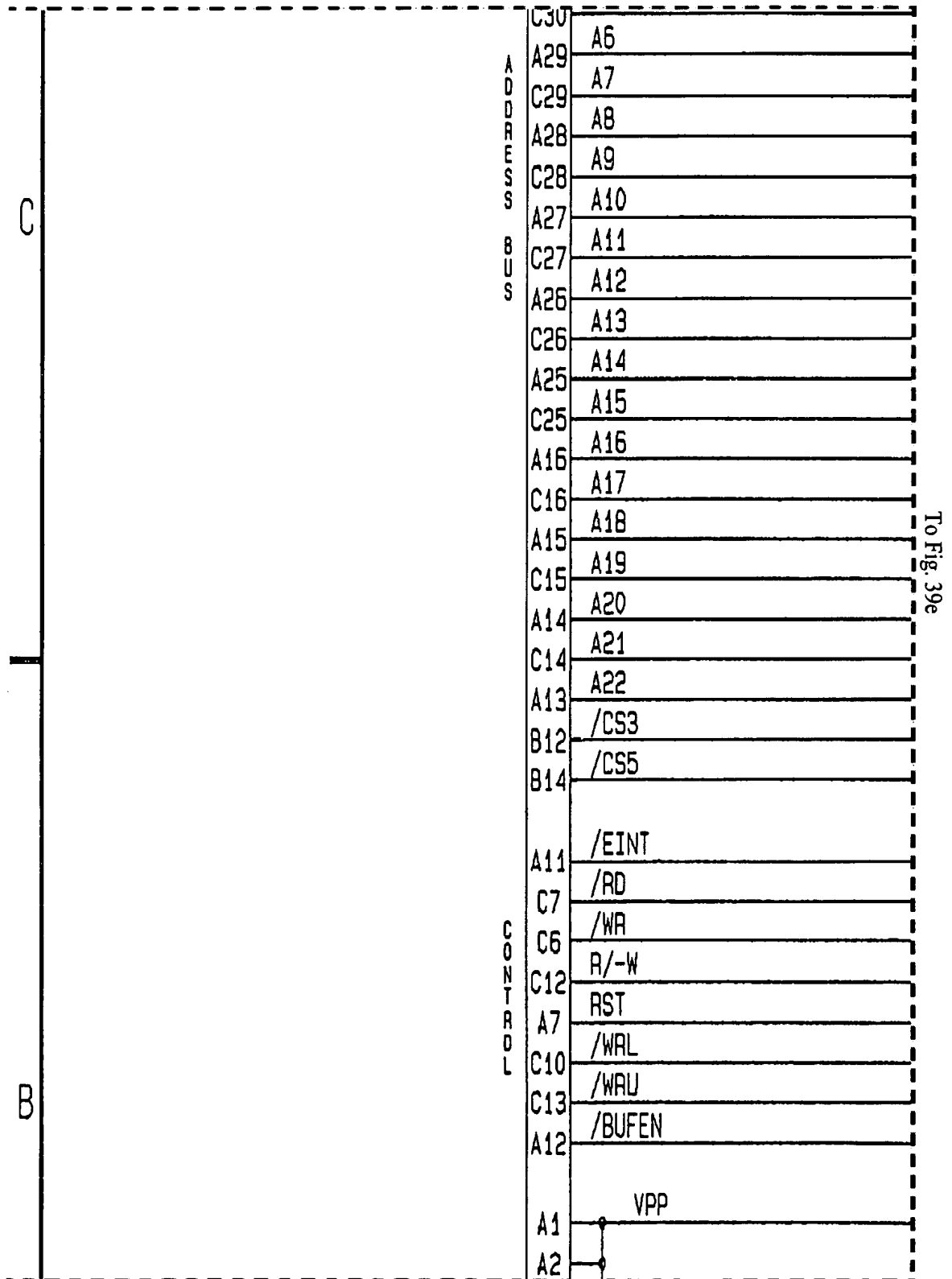








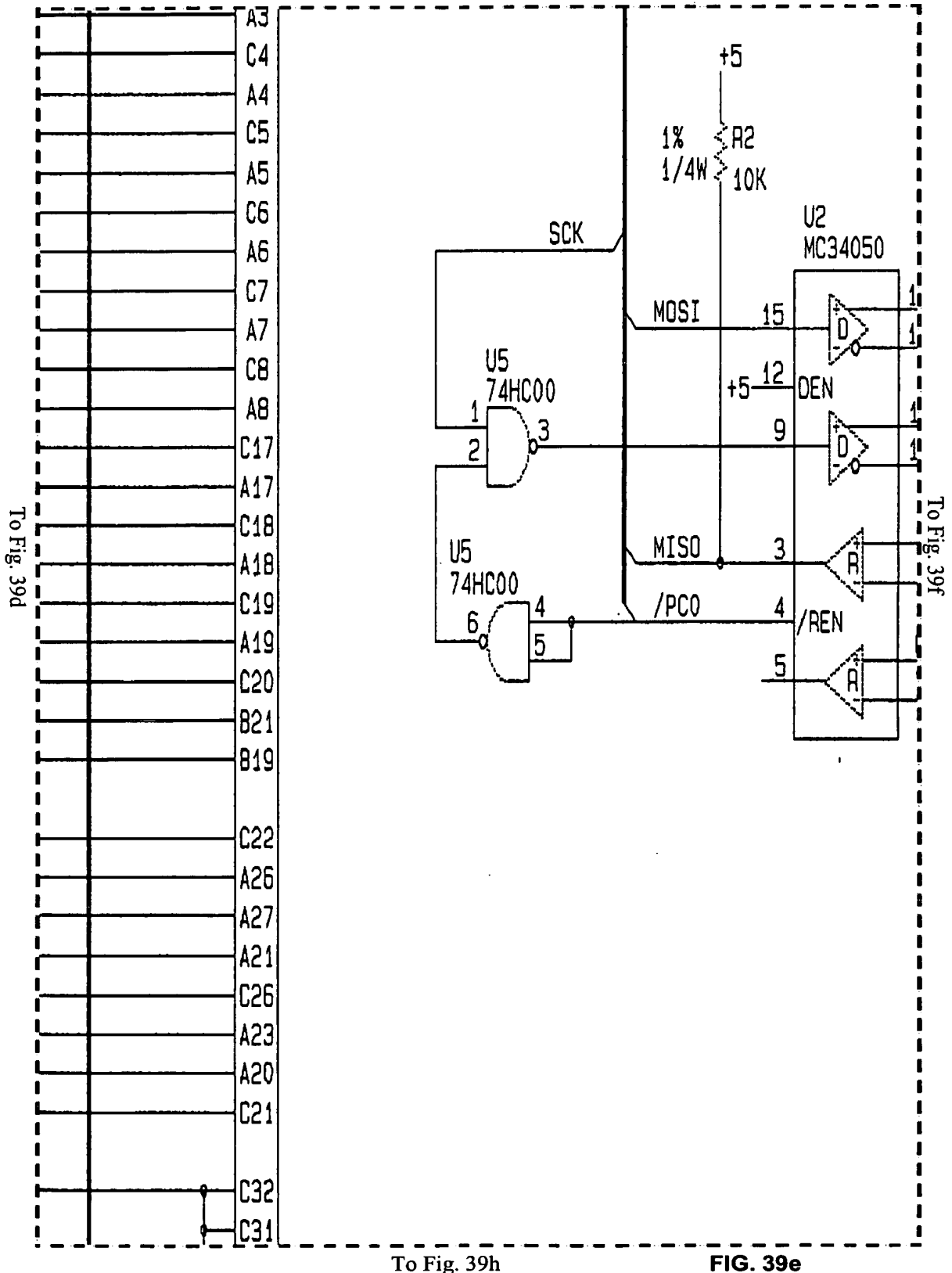
To Fig. 39a



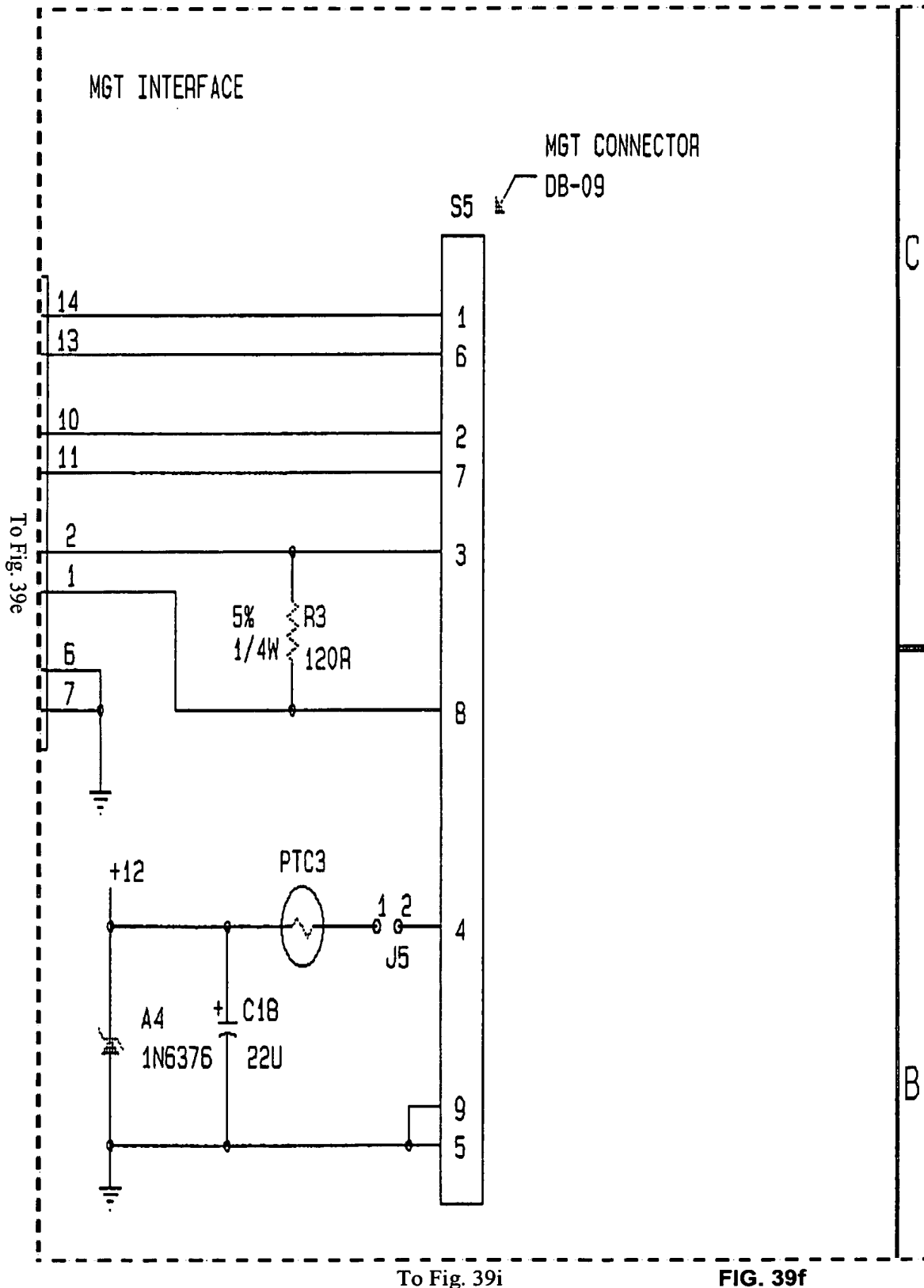
To Fig. 39g

FIG. 39d

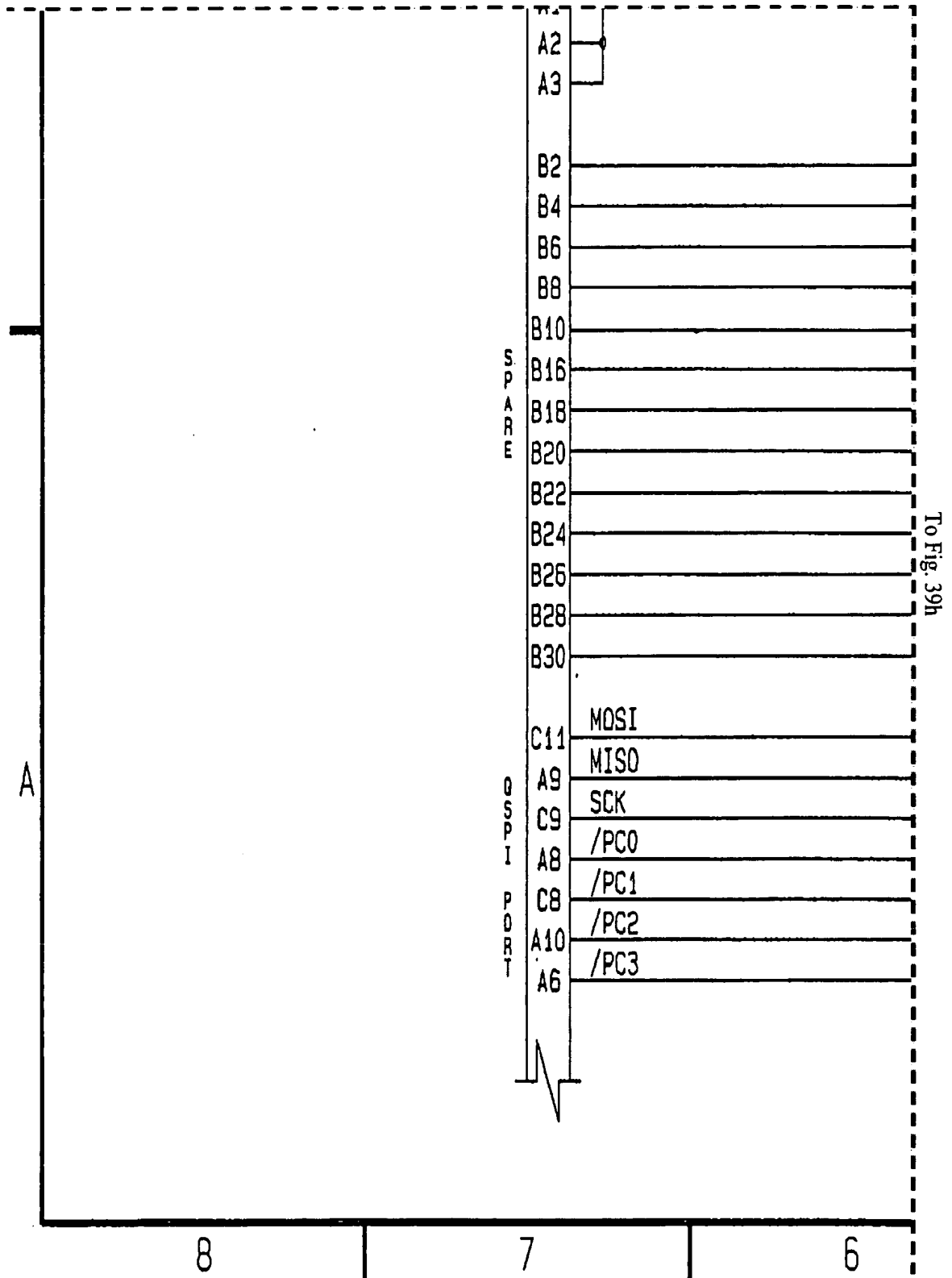
To Fig. 39b



To Fig. 39c



To Fig. 39d



To Fig. 39e

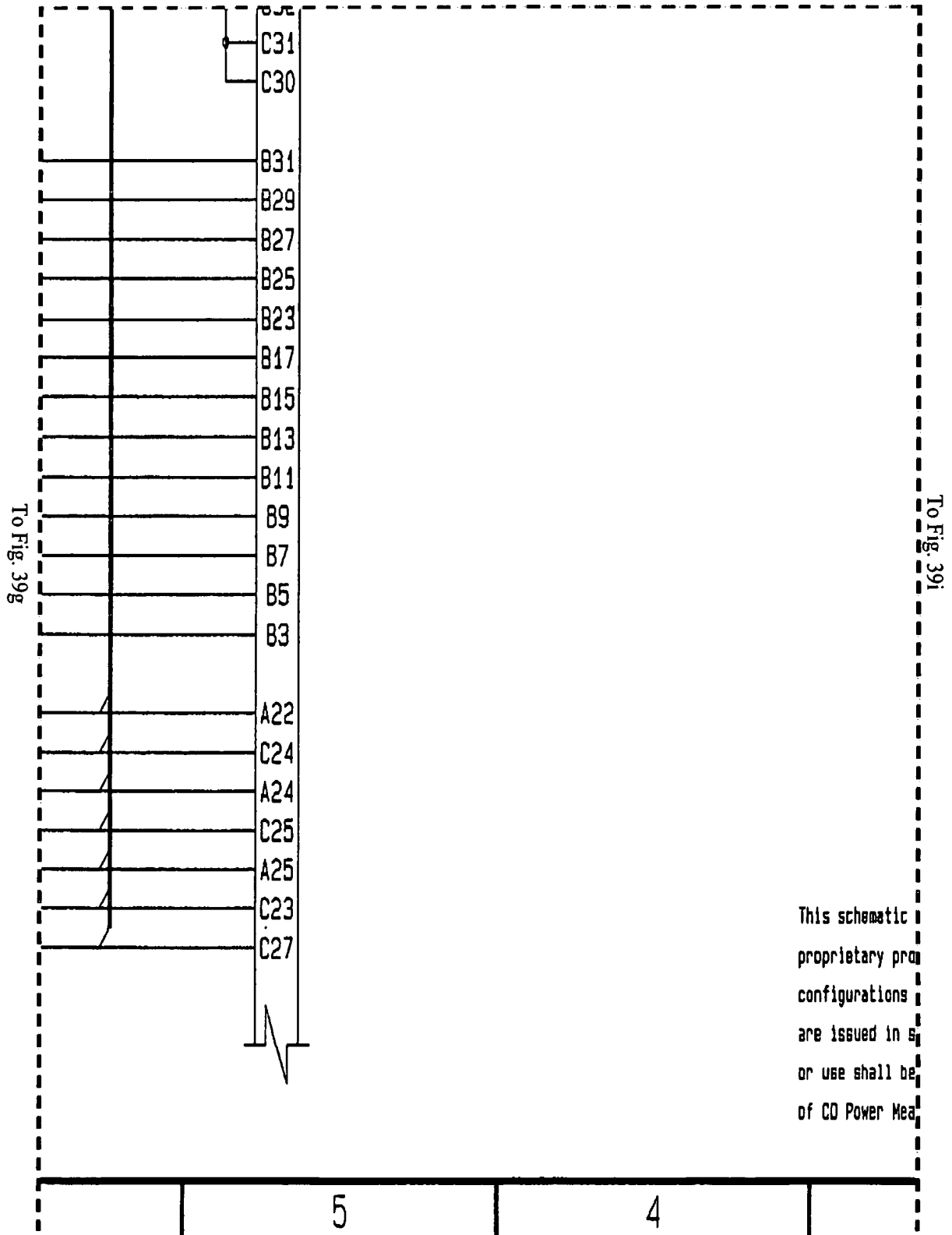


FIG. 39h



To Fig. 39f

To Fig. 39h

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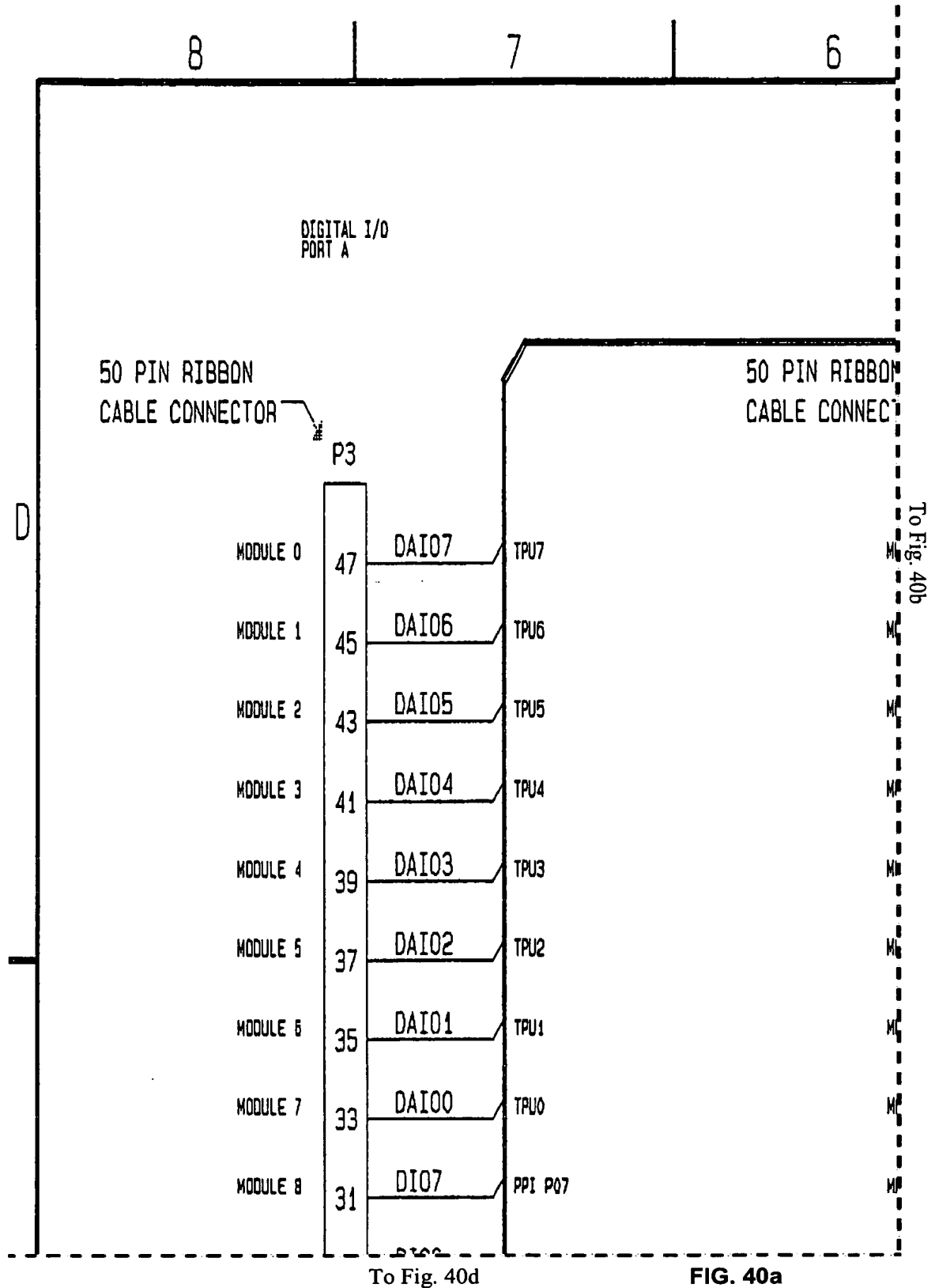
SHEET 2 OF 7

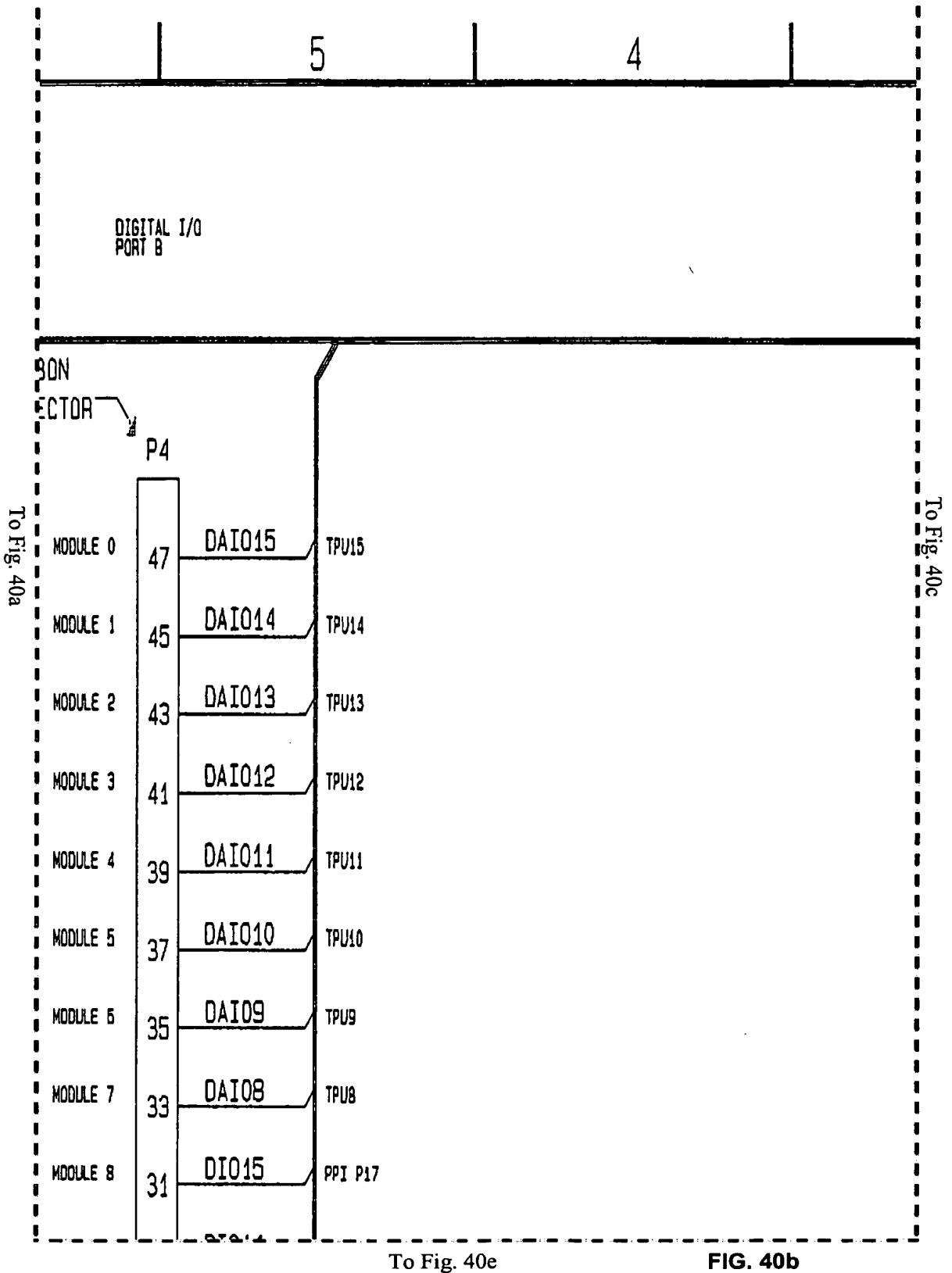
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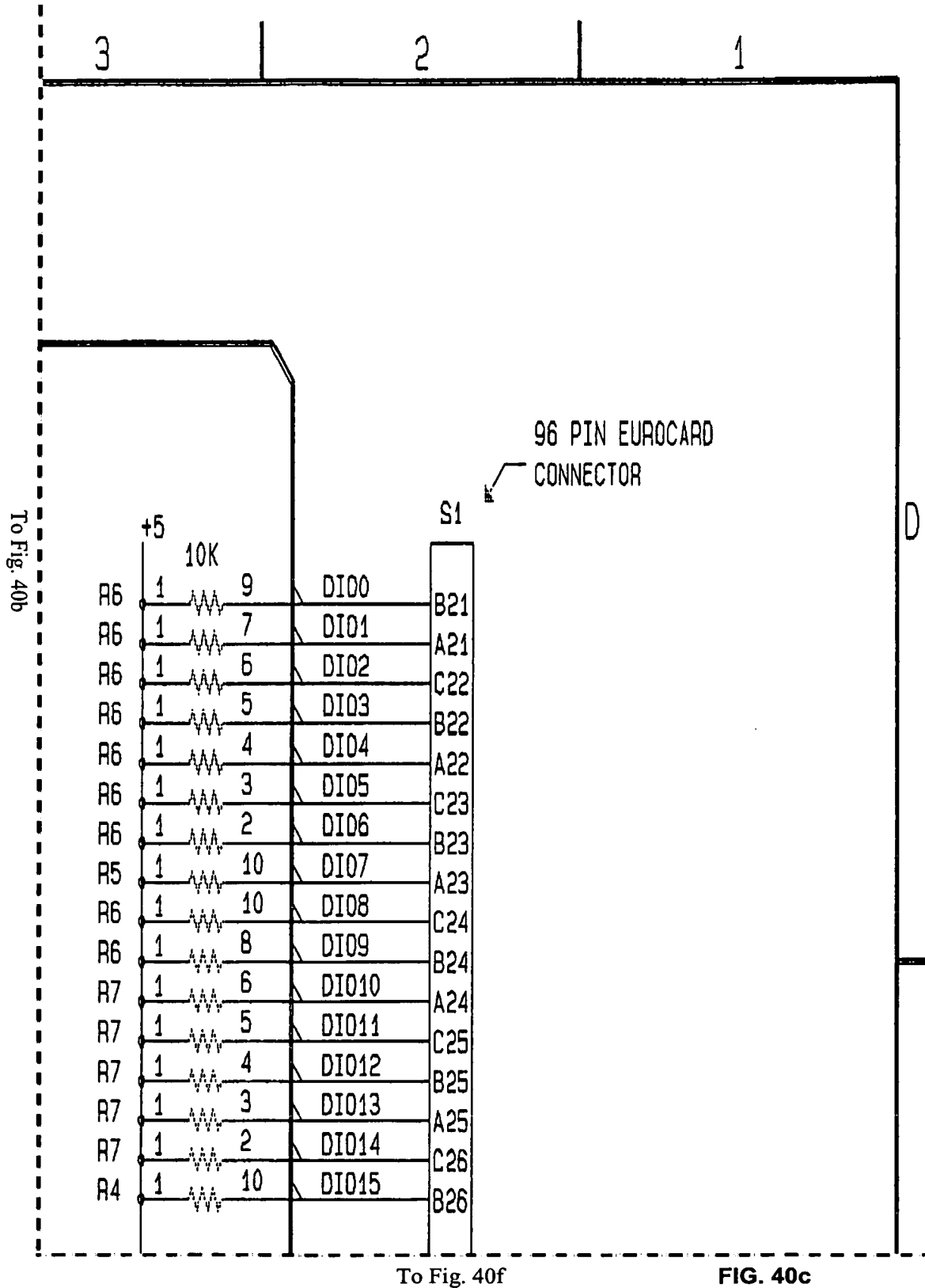
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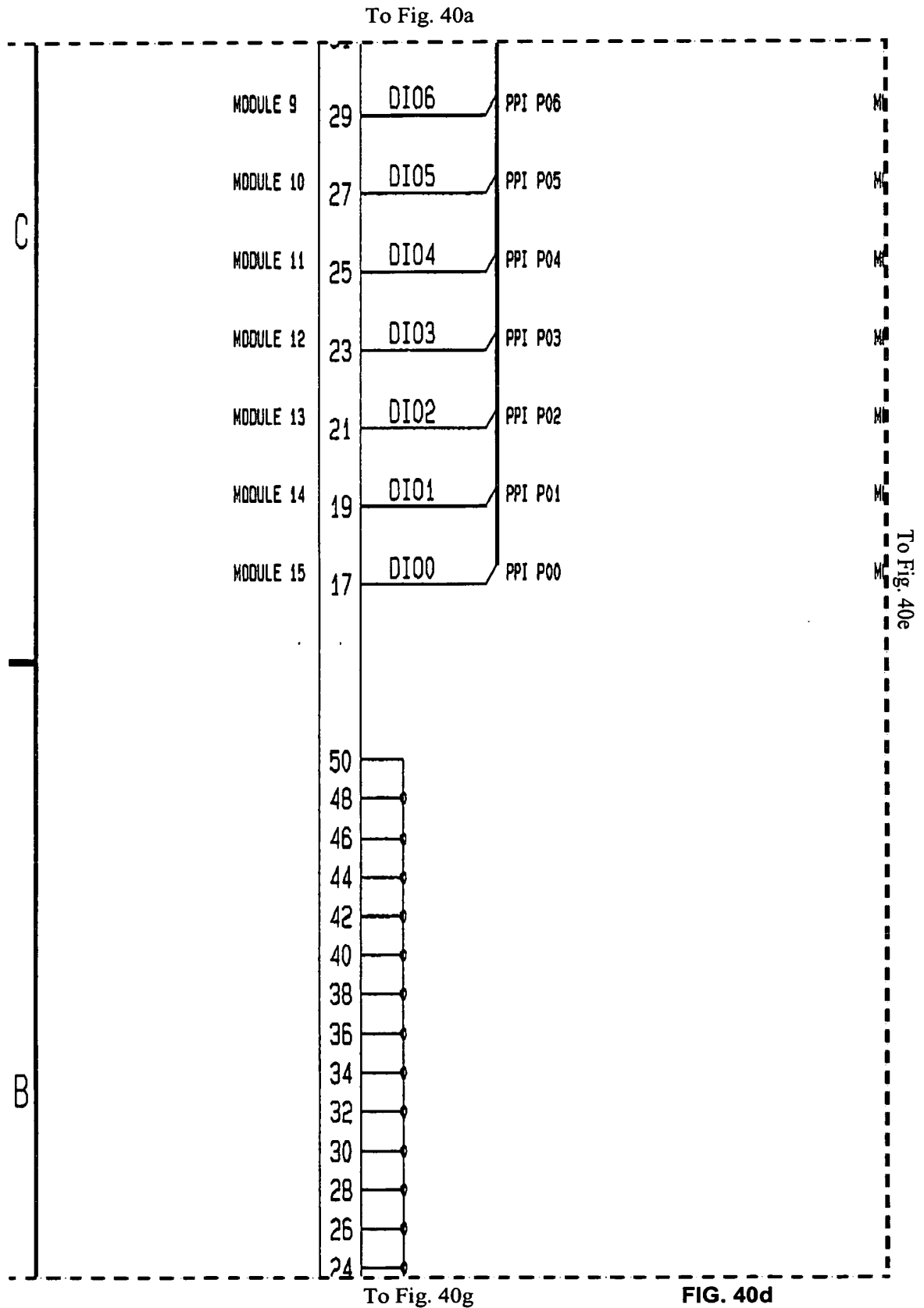
1

FIG. 39i

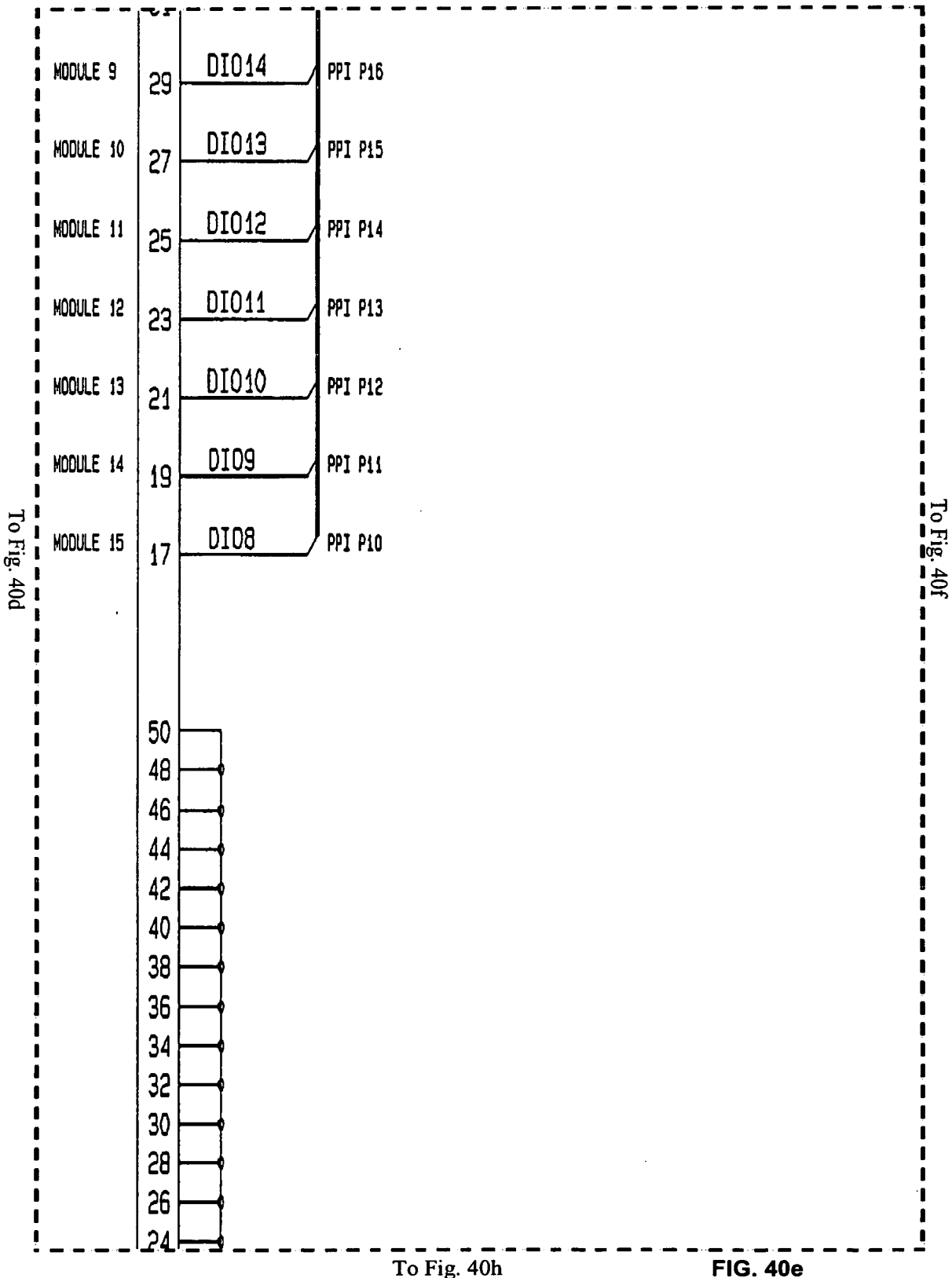




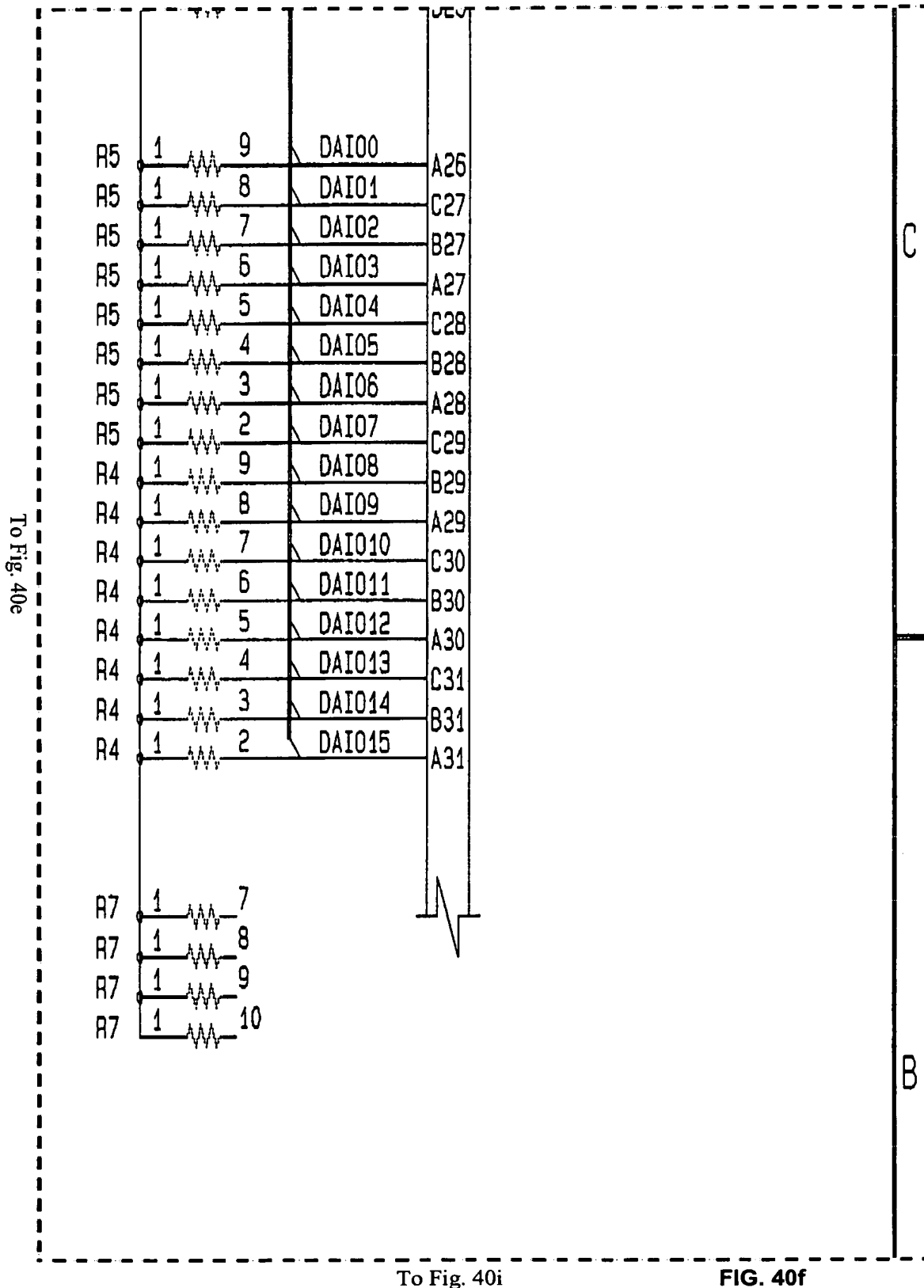




To Fig. 40b



To Fig. 40c



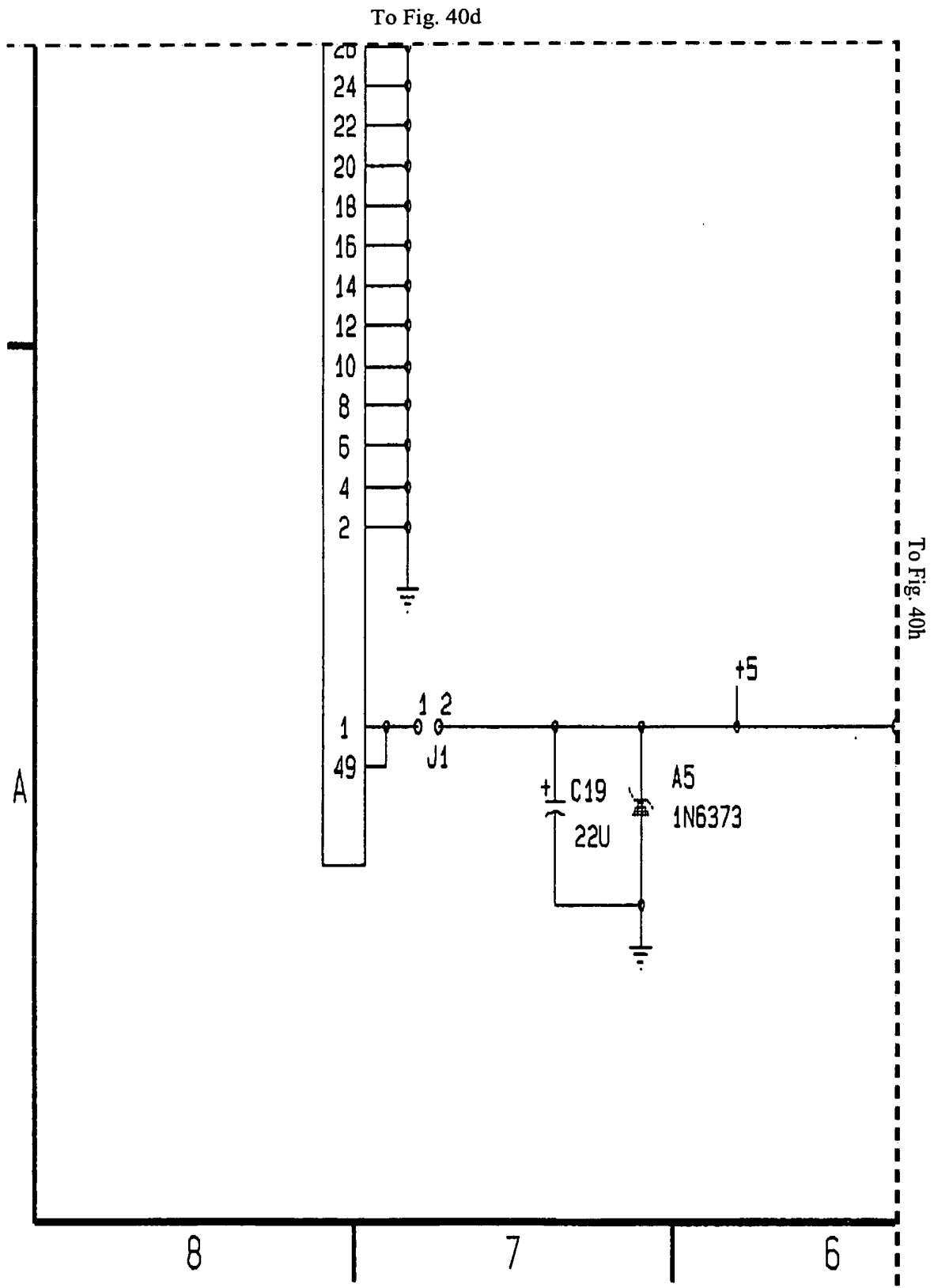
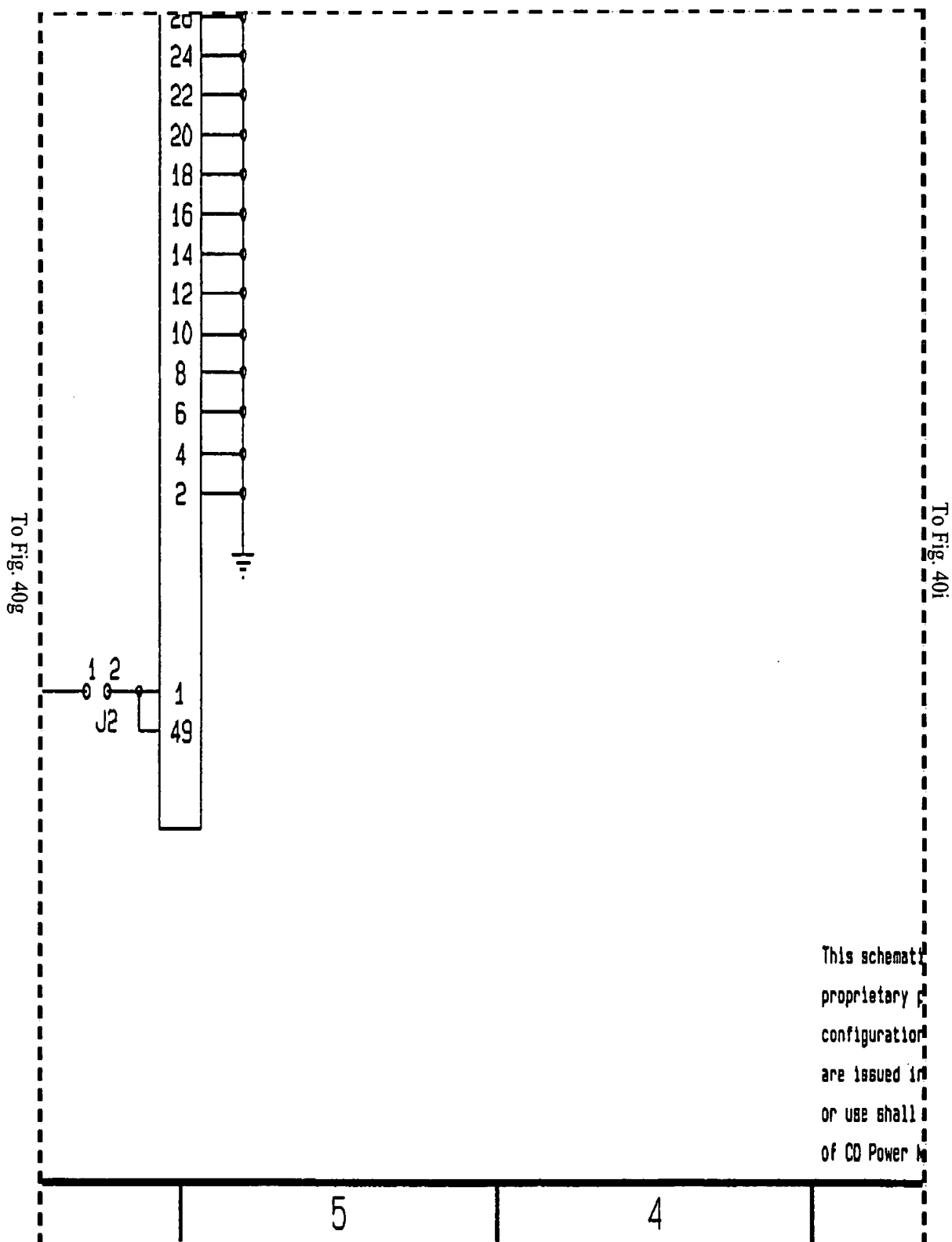


FIG. 40g



To Fig. 40e



To Fig. 40f

To Fig. 40h

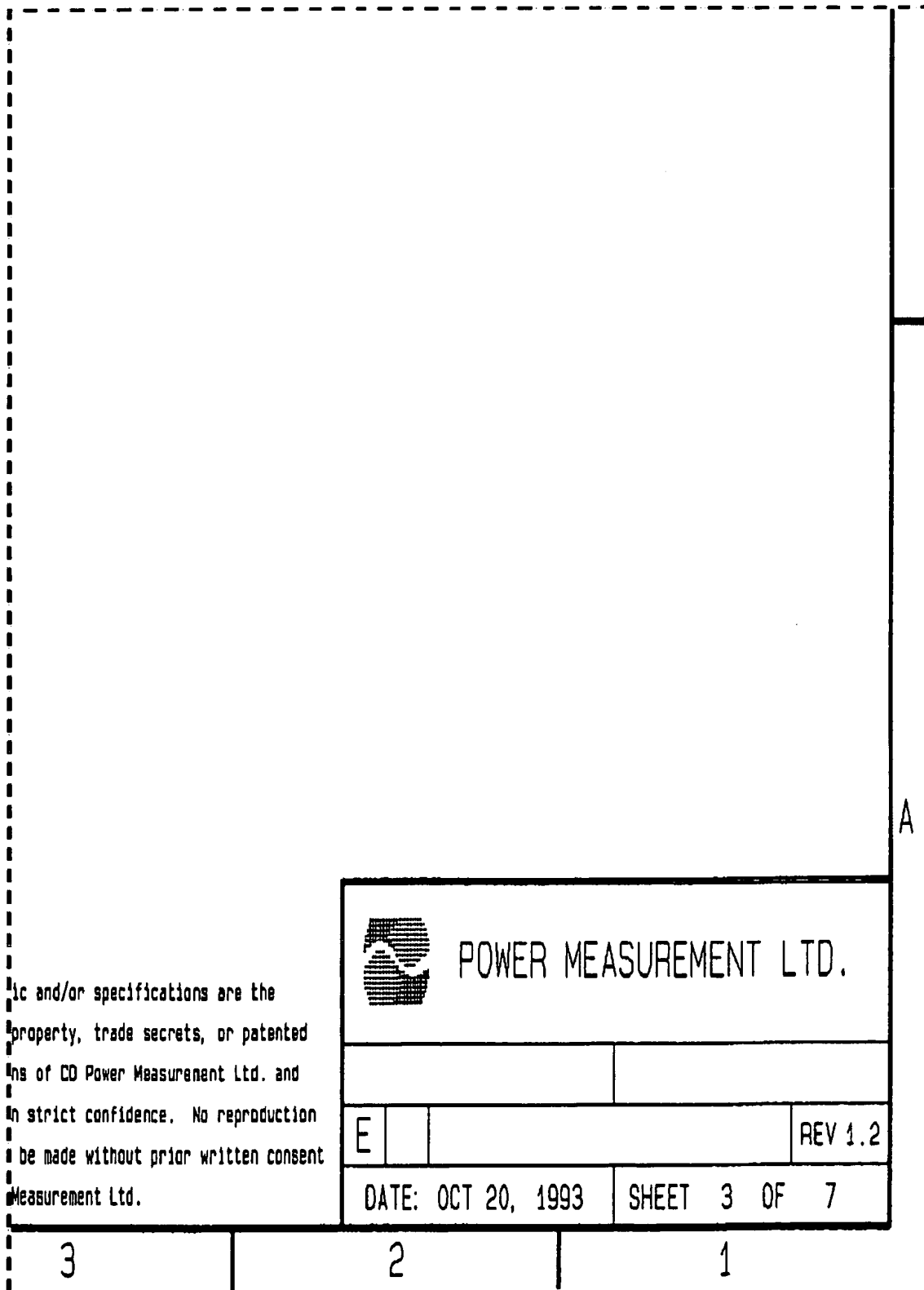
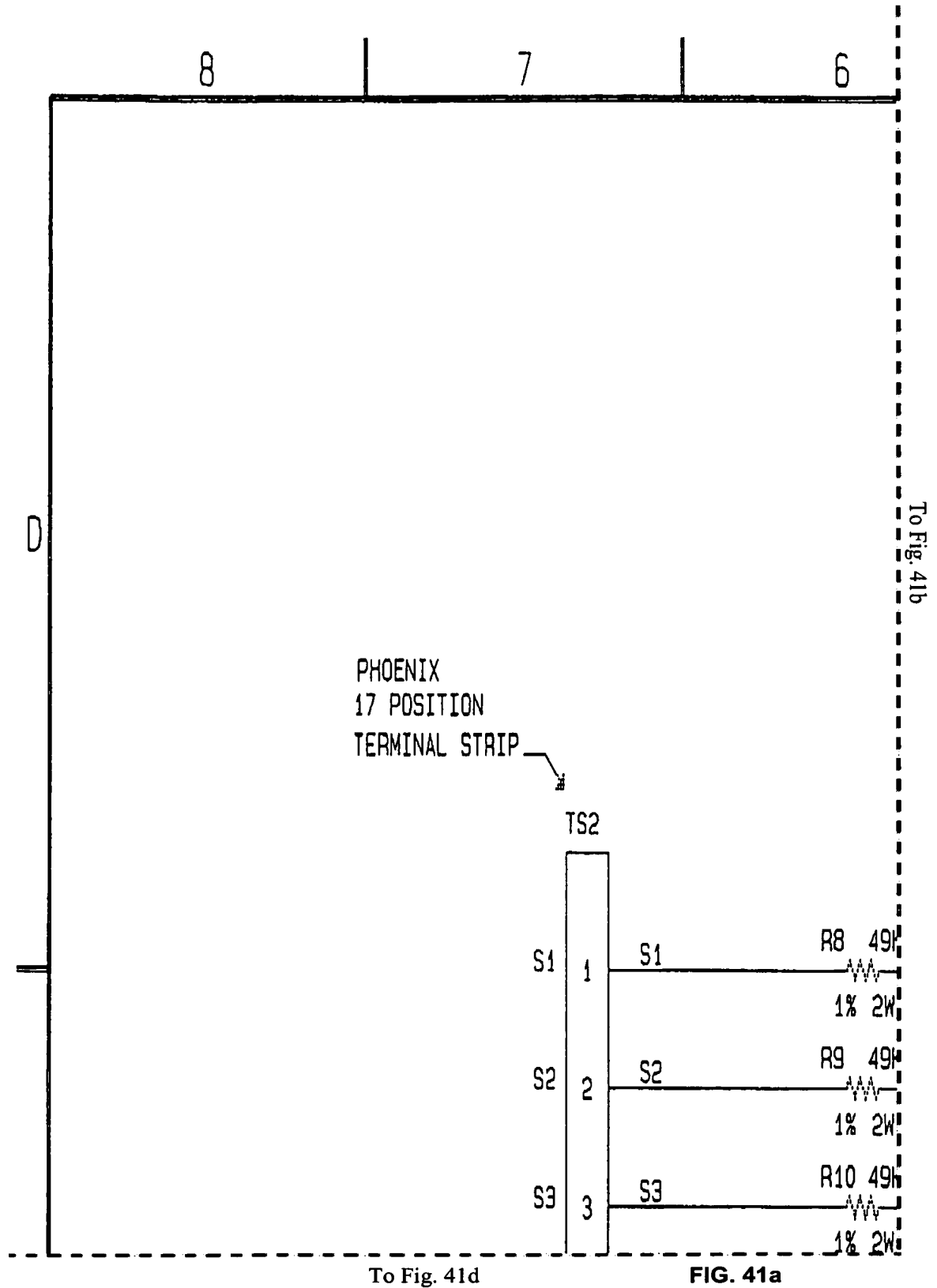
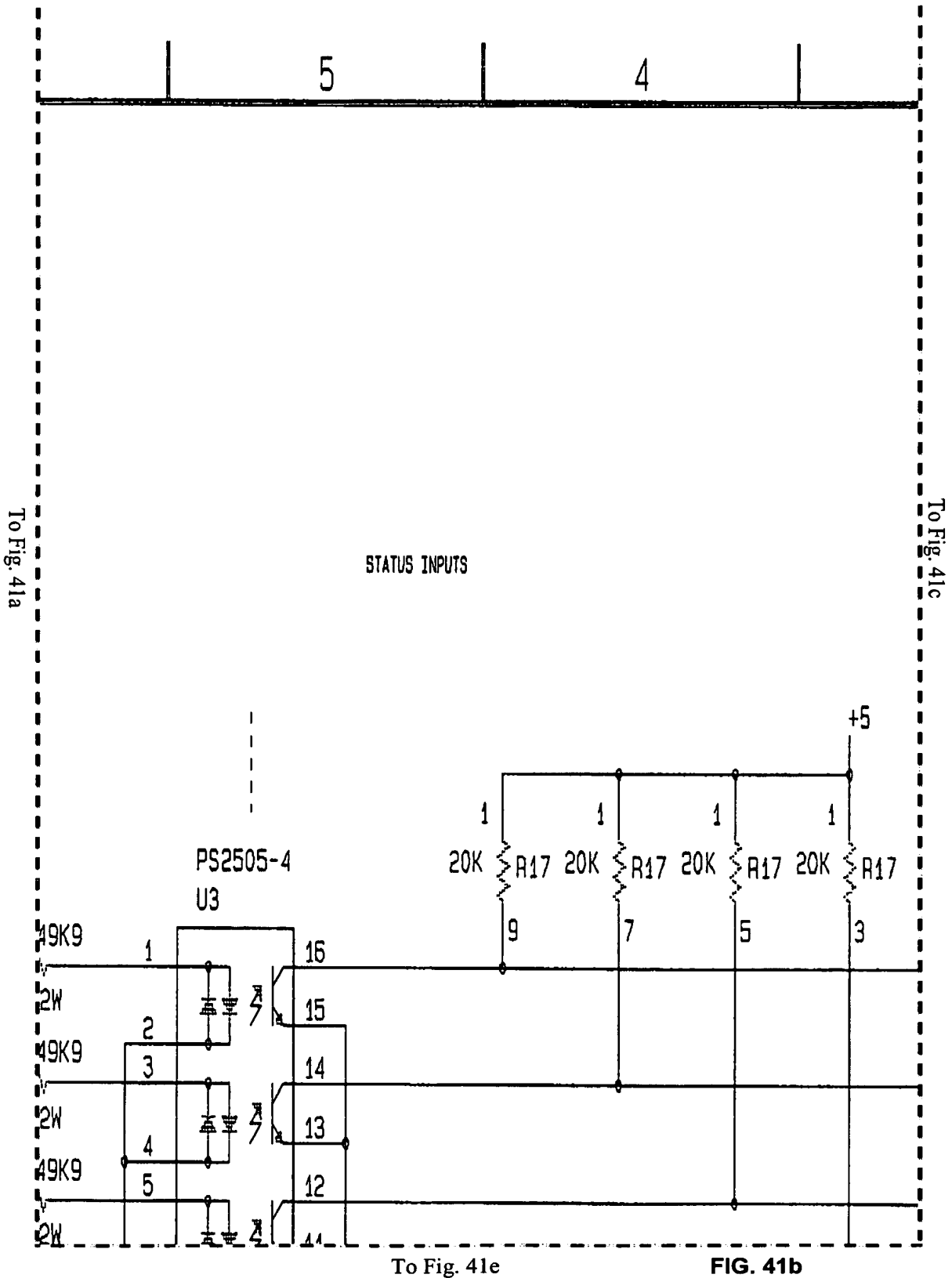
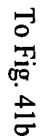


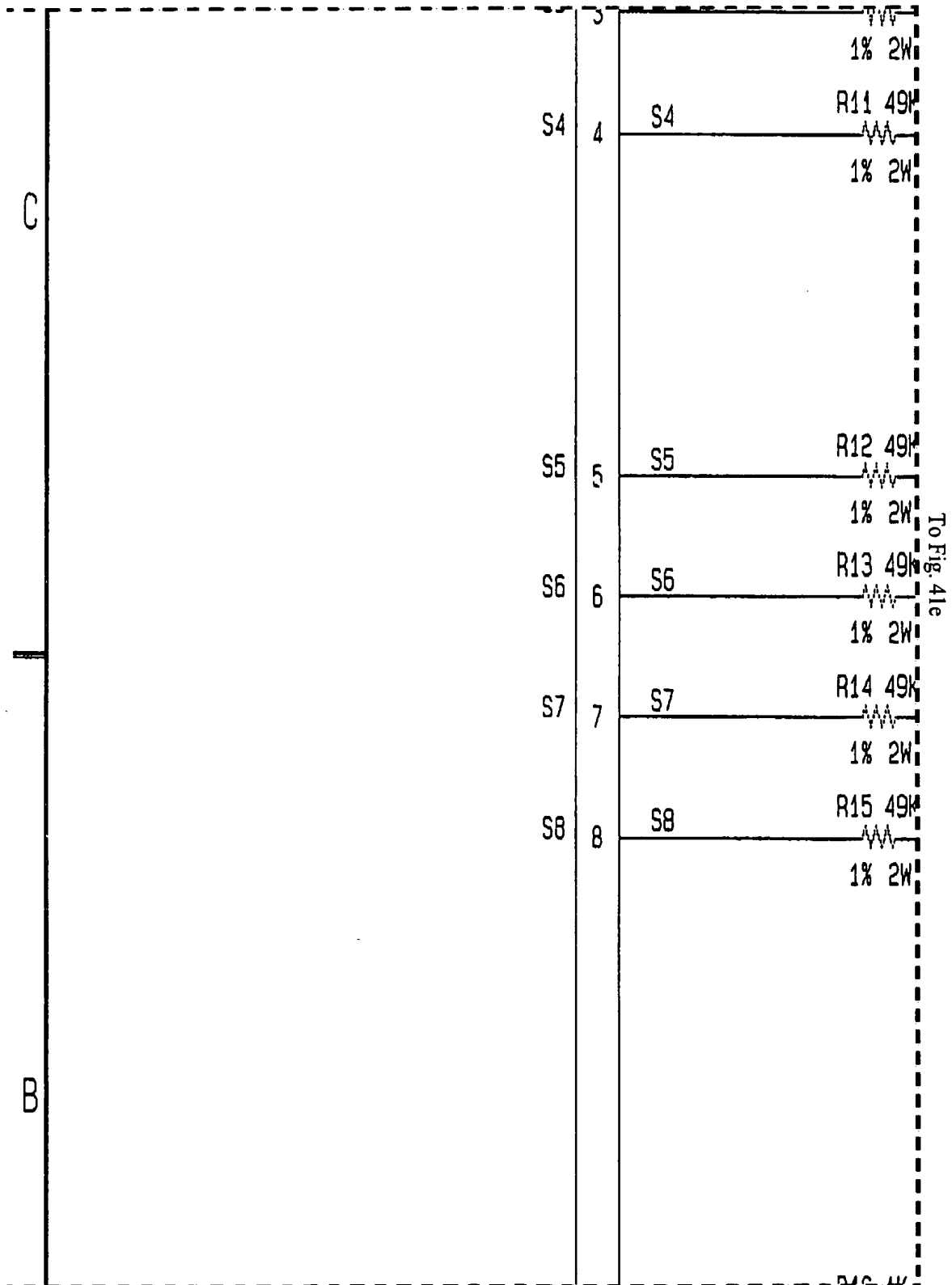
FIG. 40i







To Fig. 41a



To Fig. 41g

FIG. 41d

To Fig. 41b

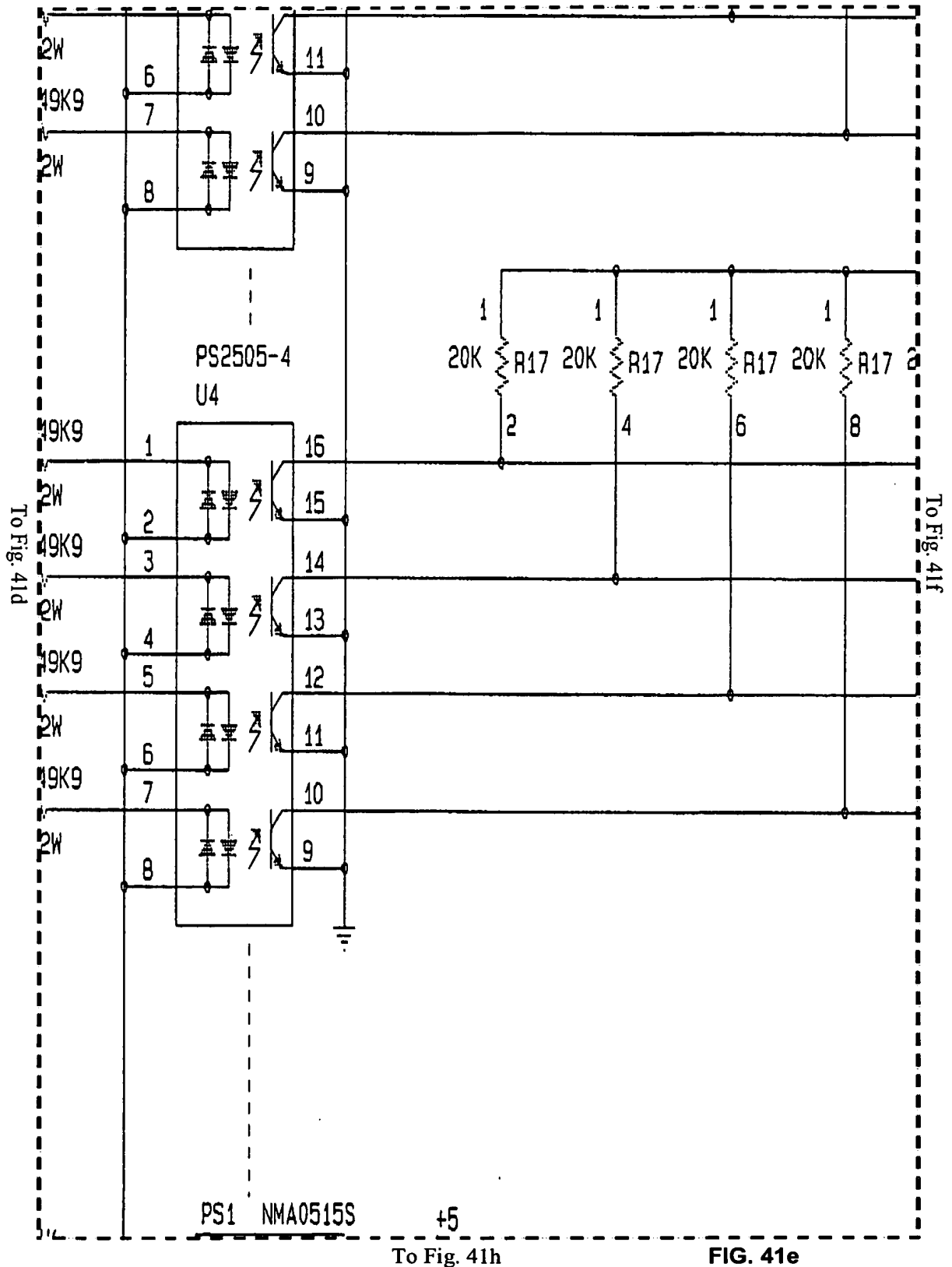
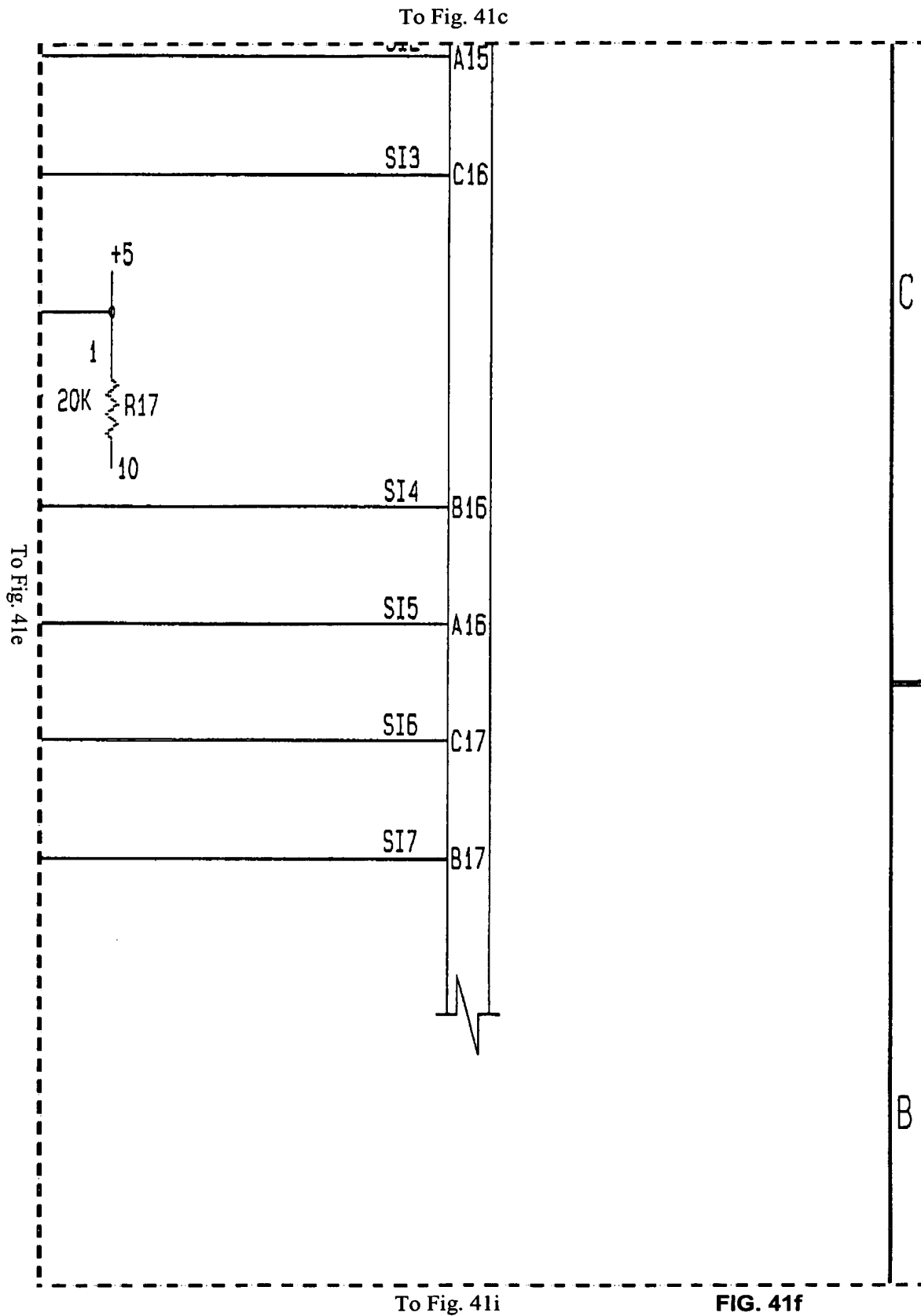
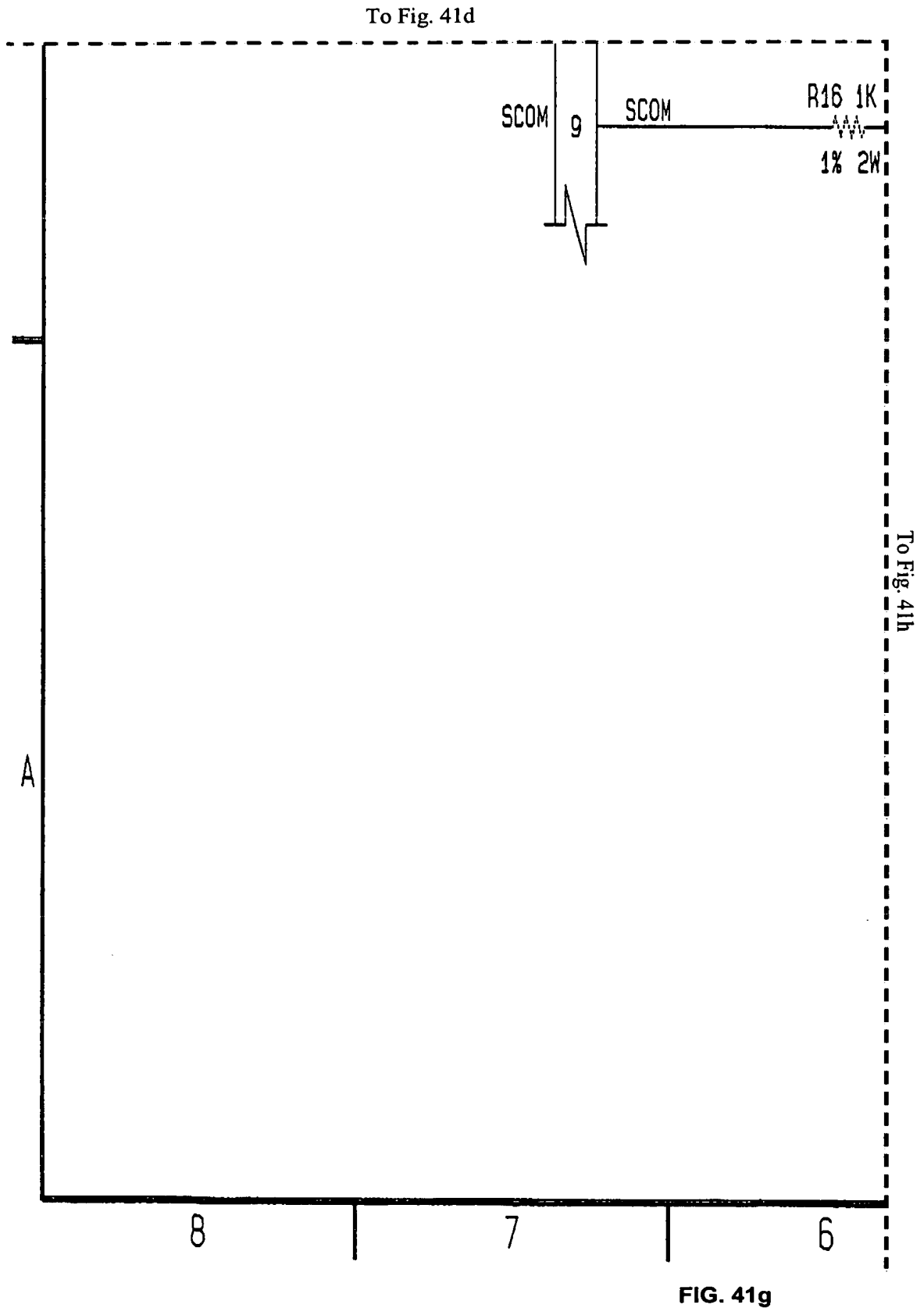
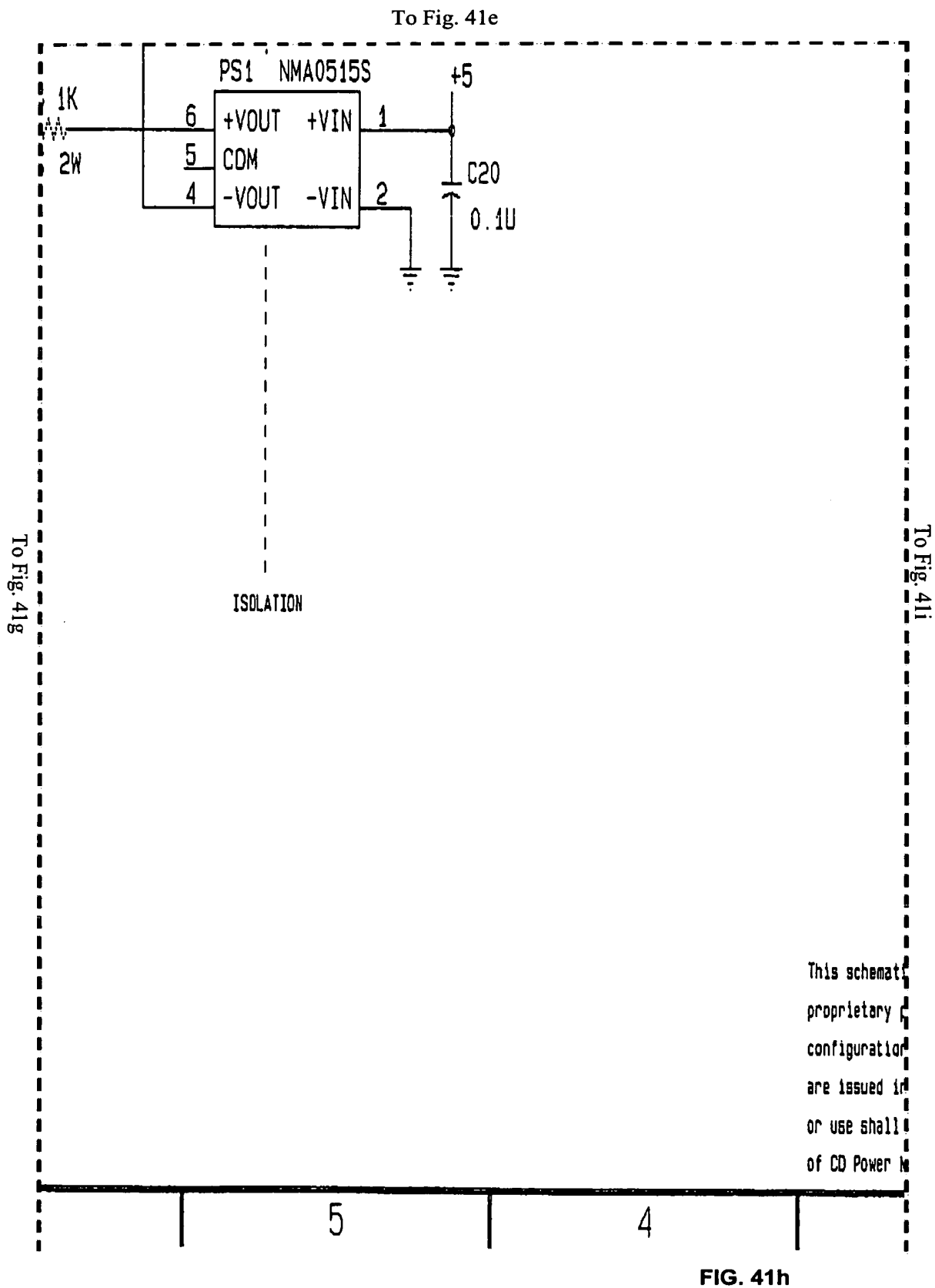


FIG. 41e









To Fig. 41f

To Fig. 41h

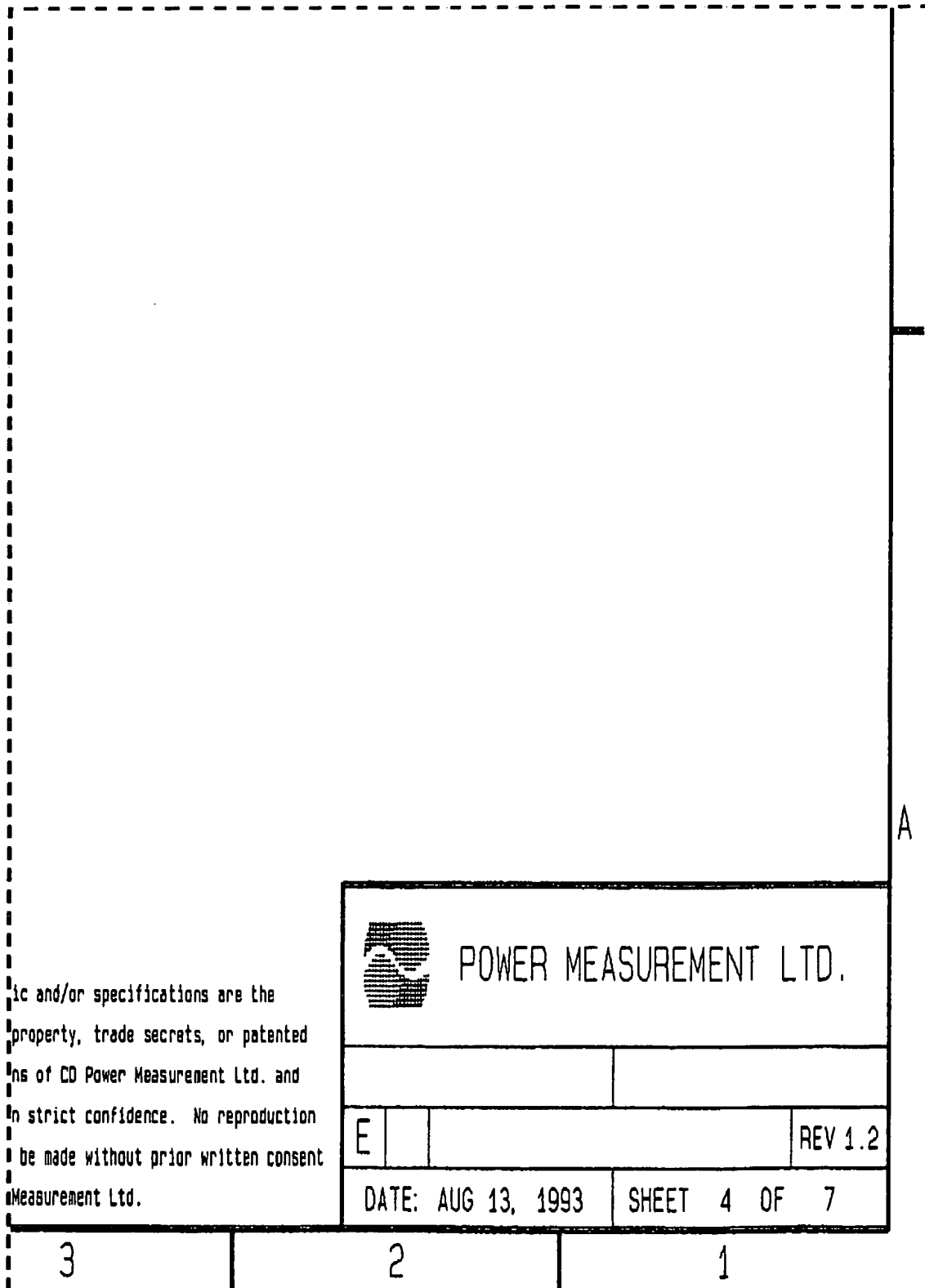
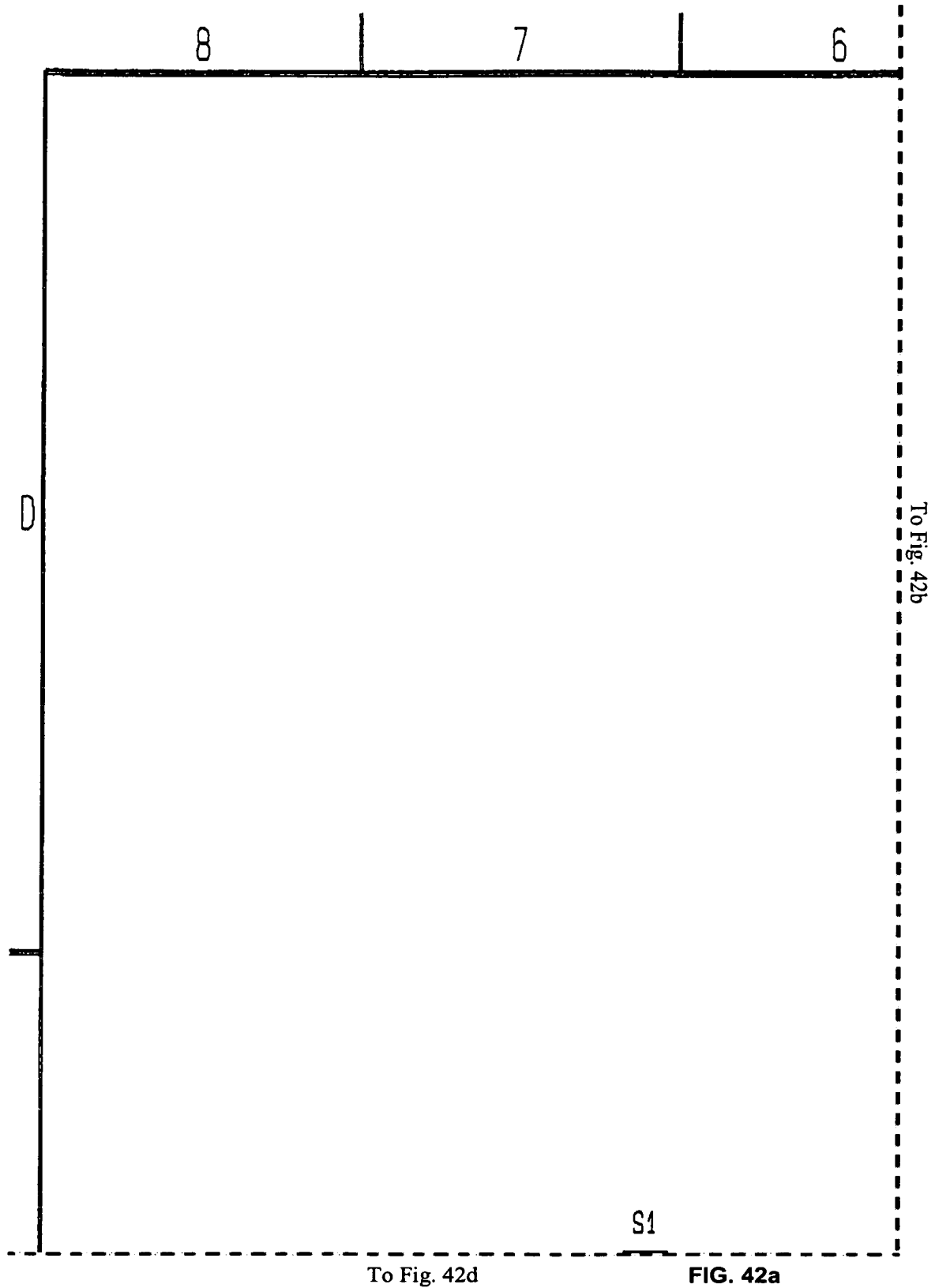
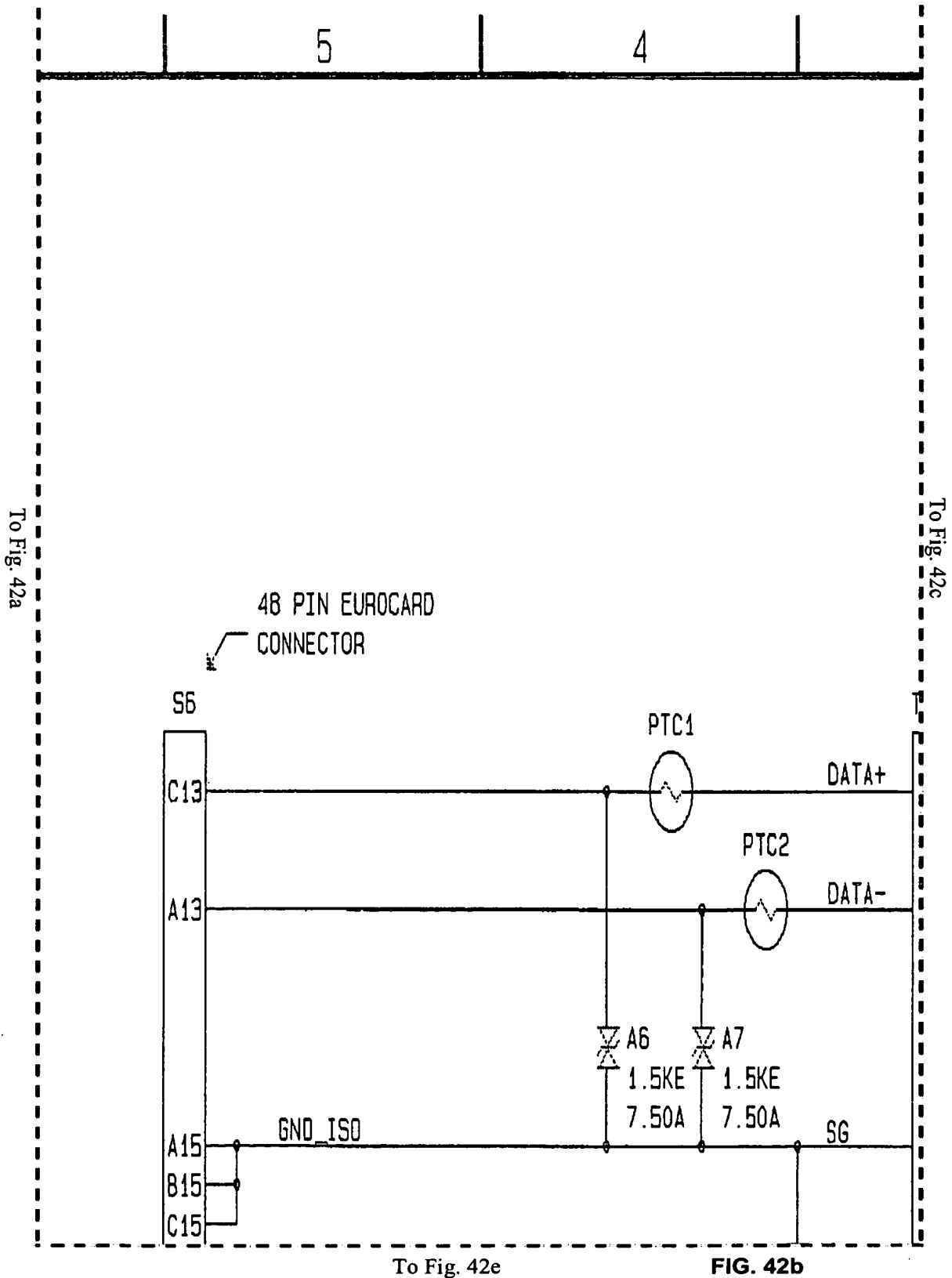
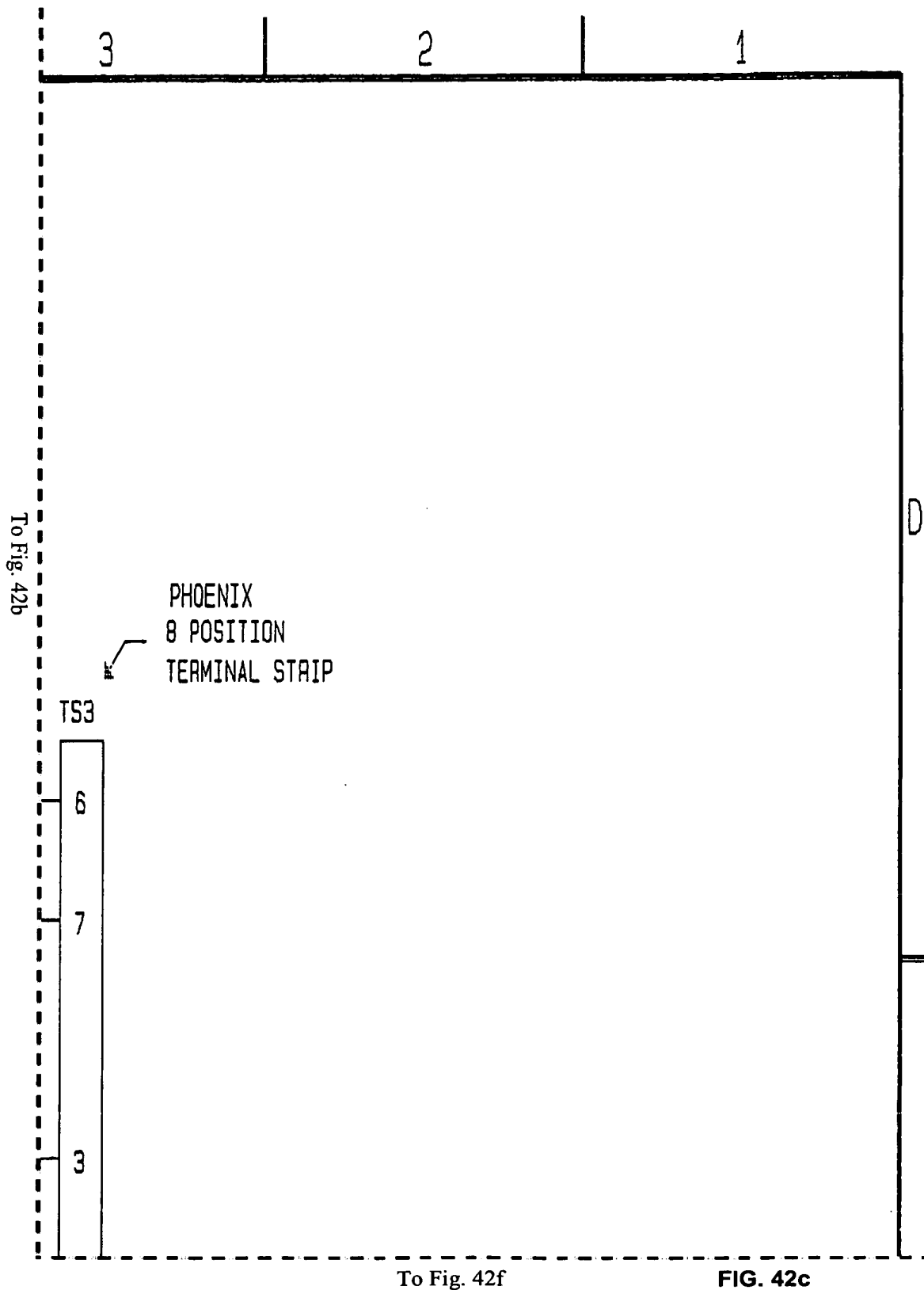


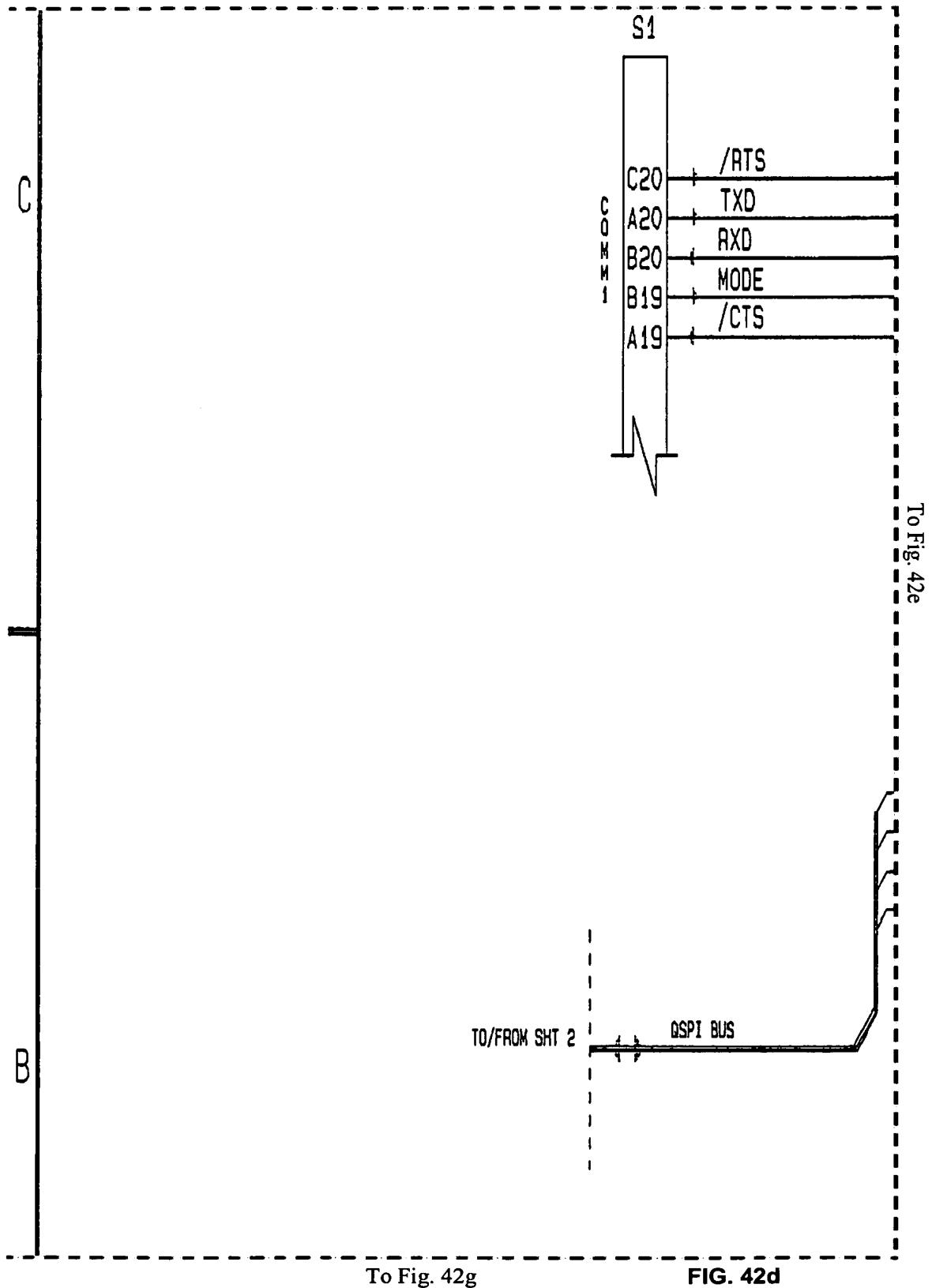
FIG. 41i



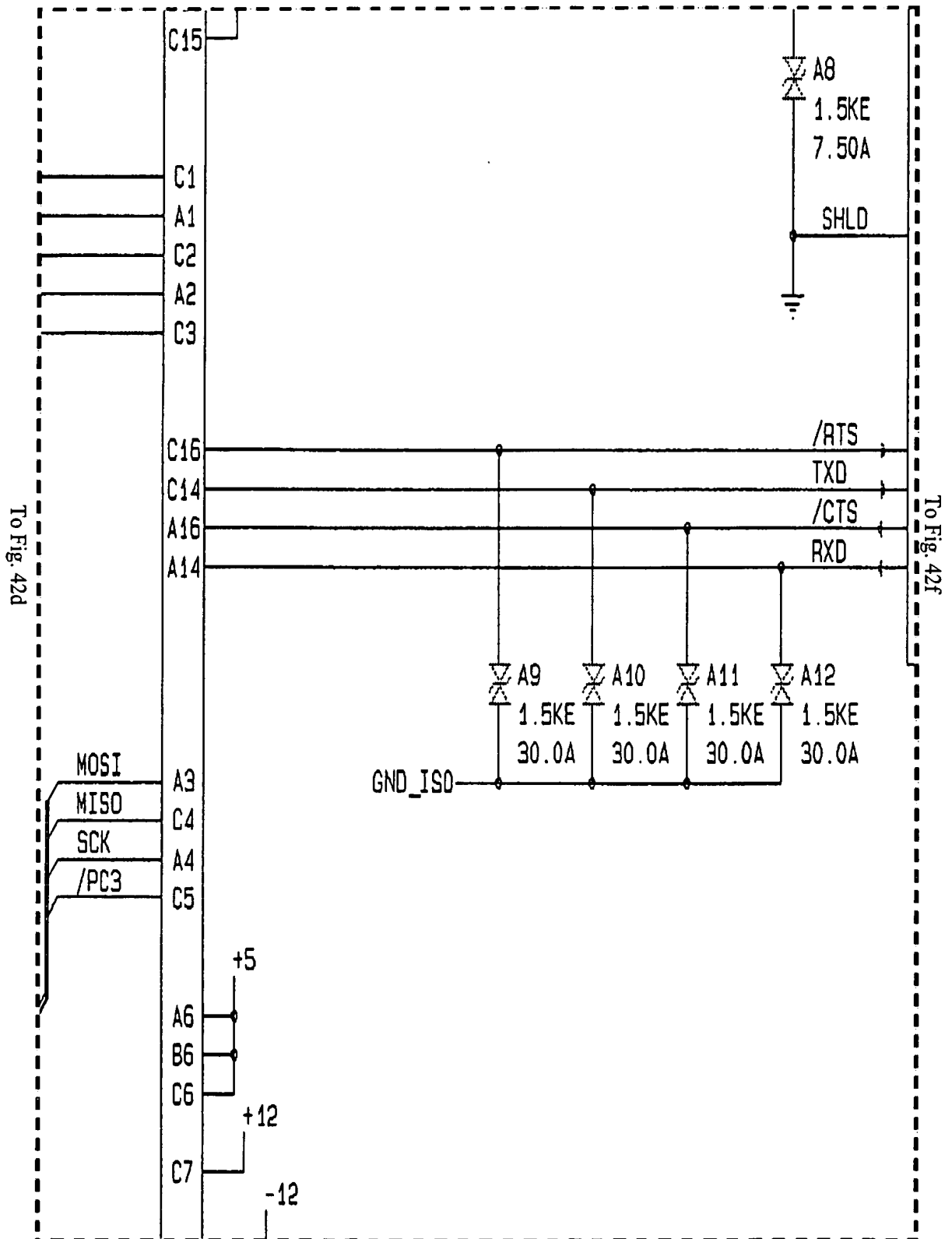




To Fig. 42a

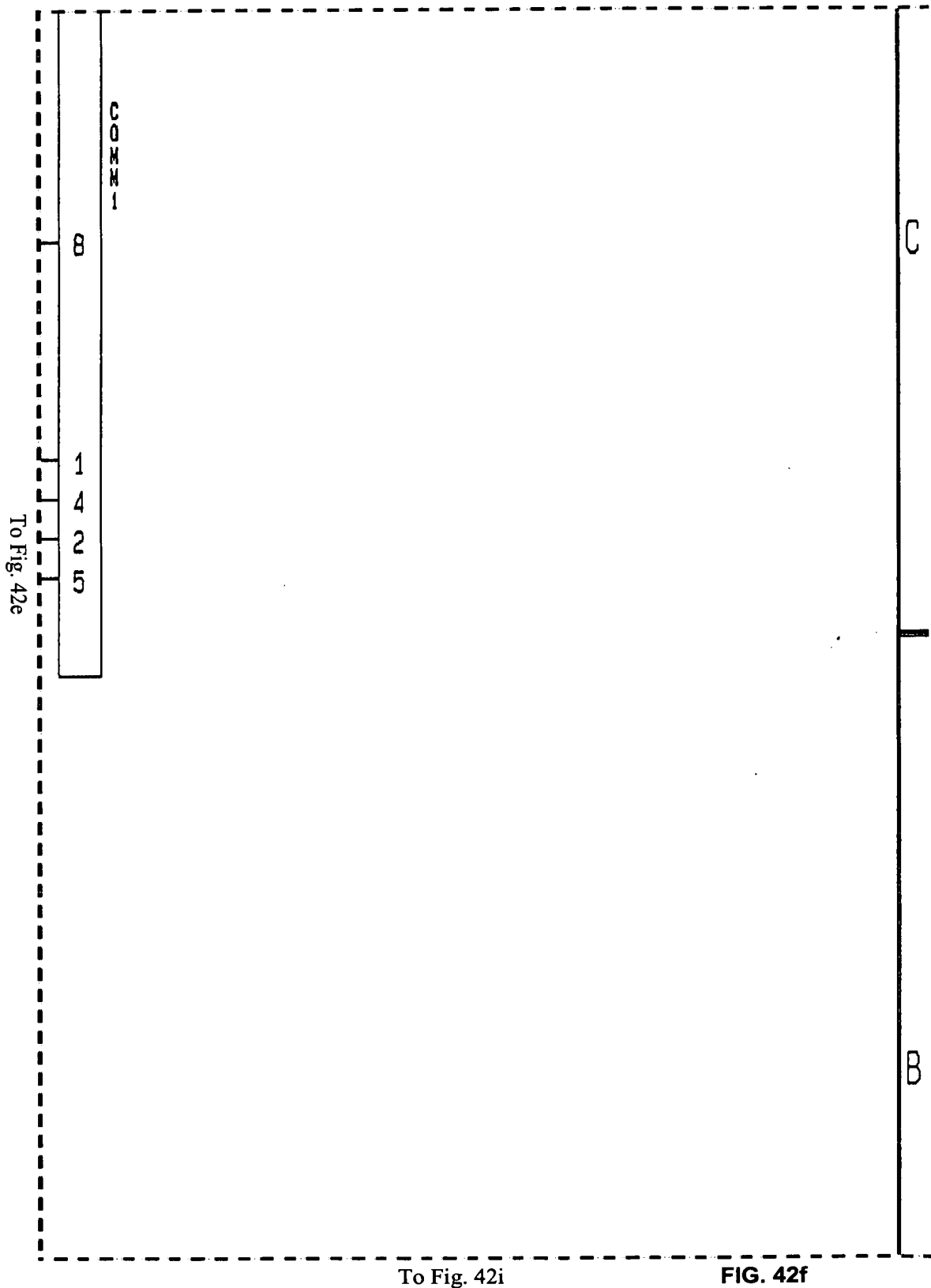


To Fig. 42b





To Fig. 42c



To Fig. 42d

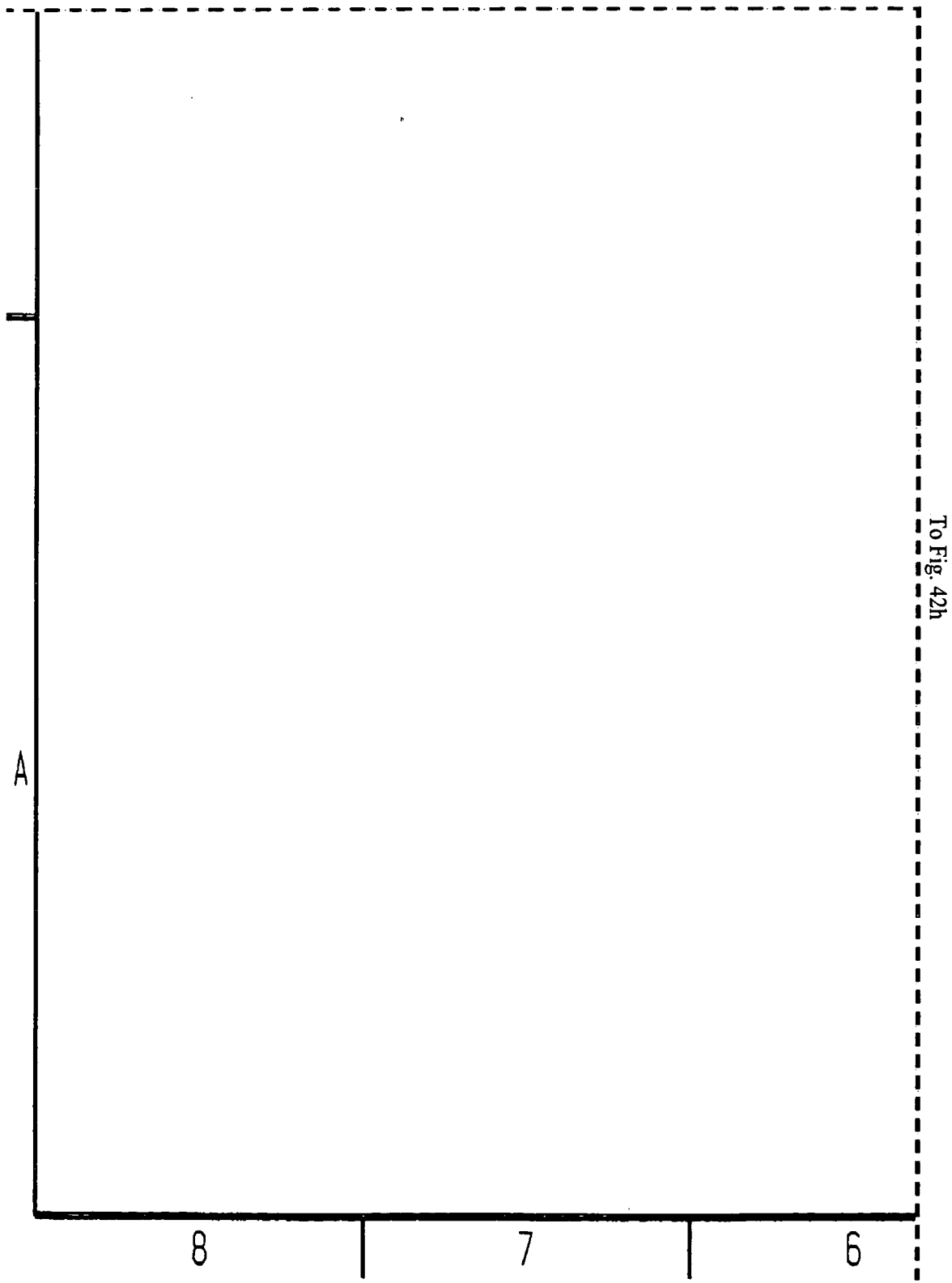


FIG. 42g

To Fig. 42e

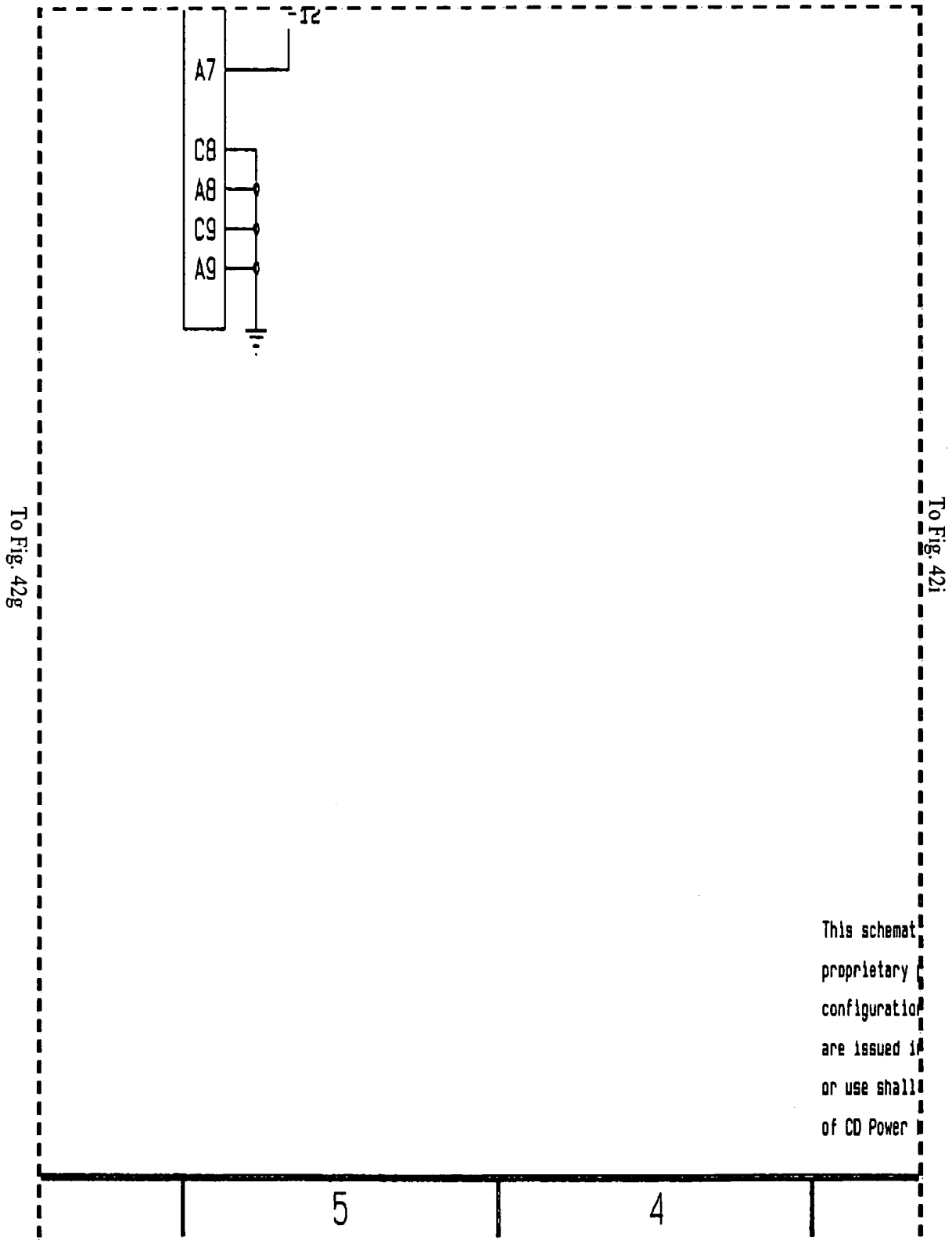
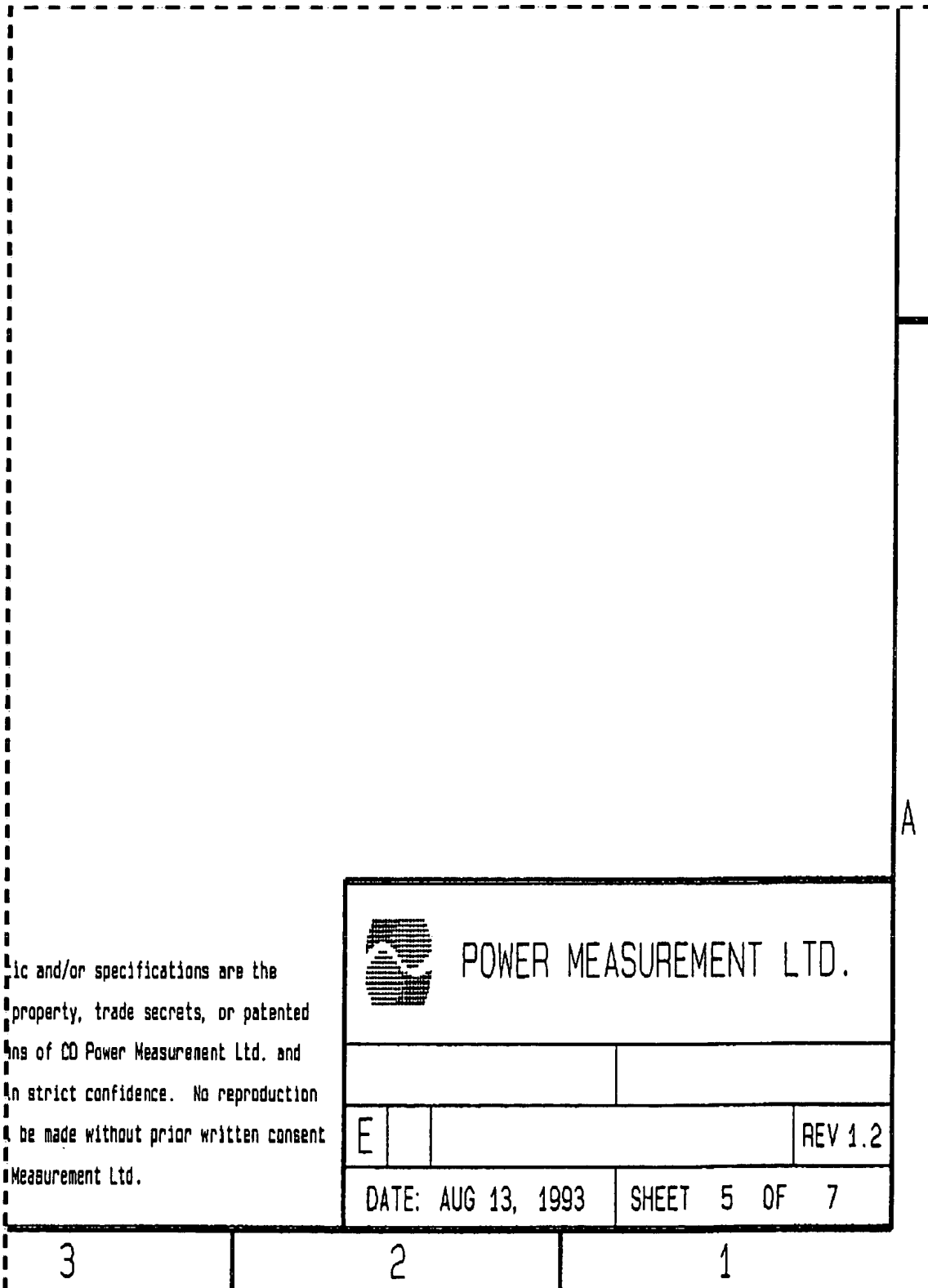


FIG. 42h

To Fig. 42f

To Fig. 42h



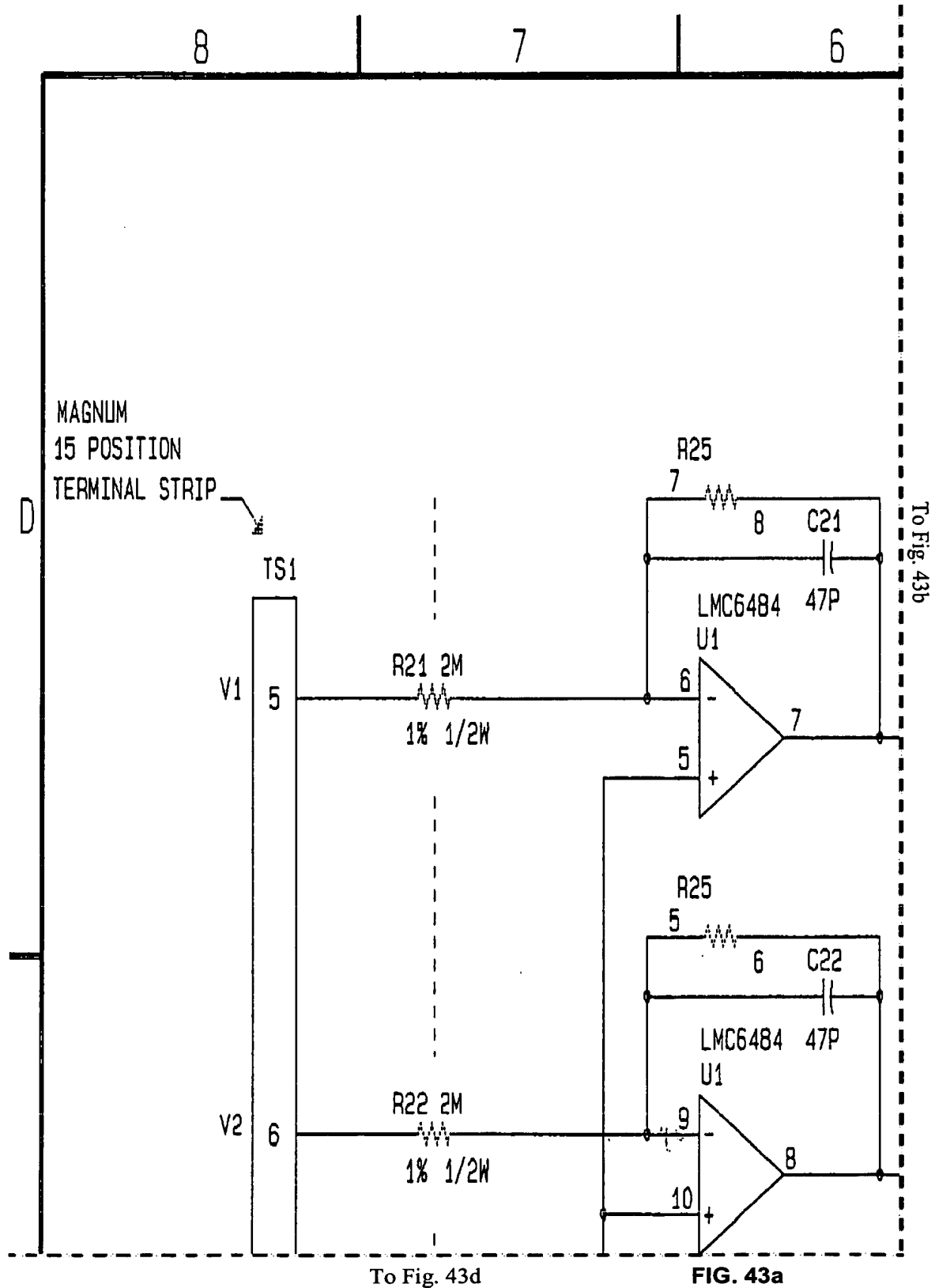
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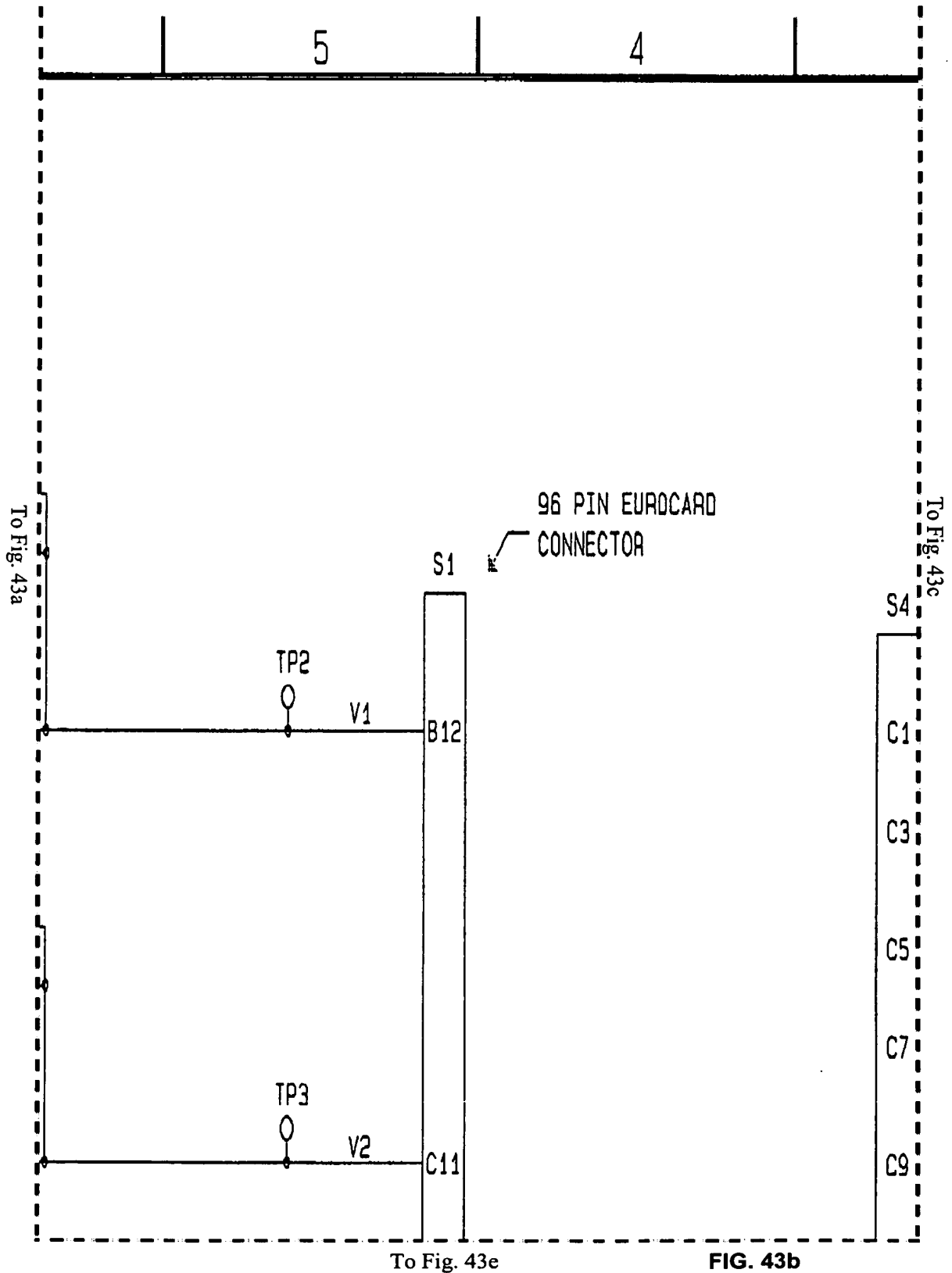
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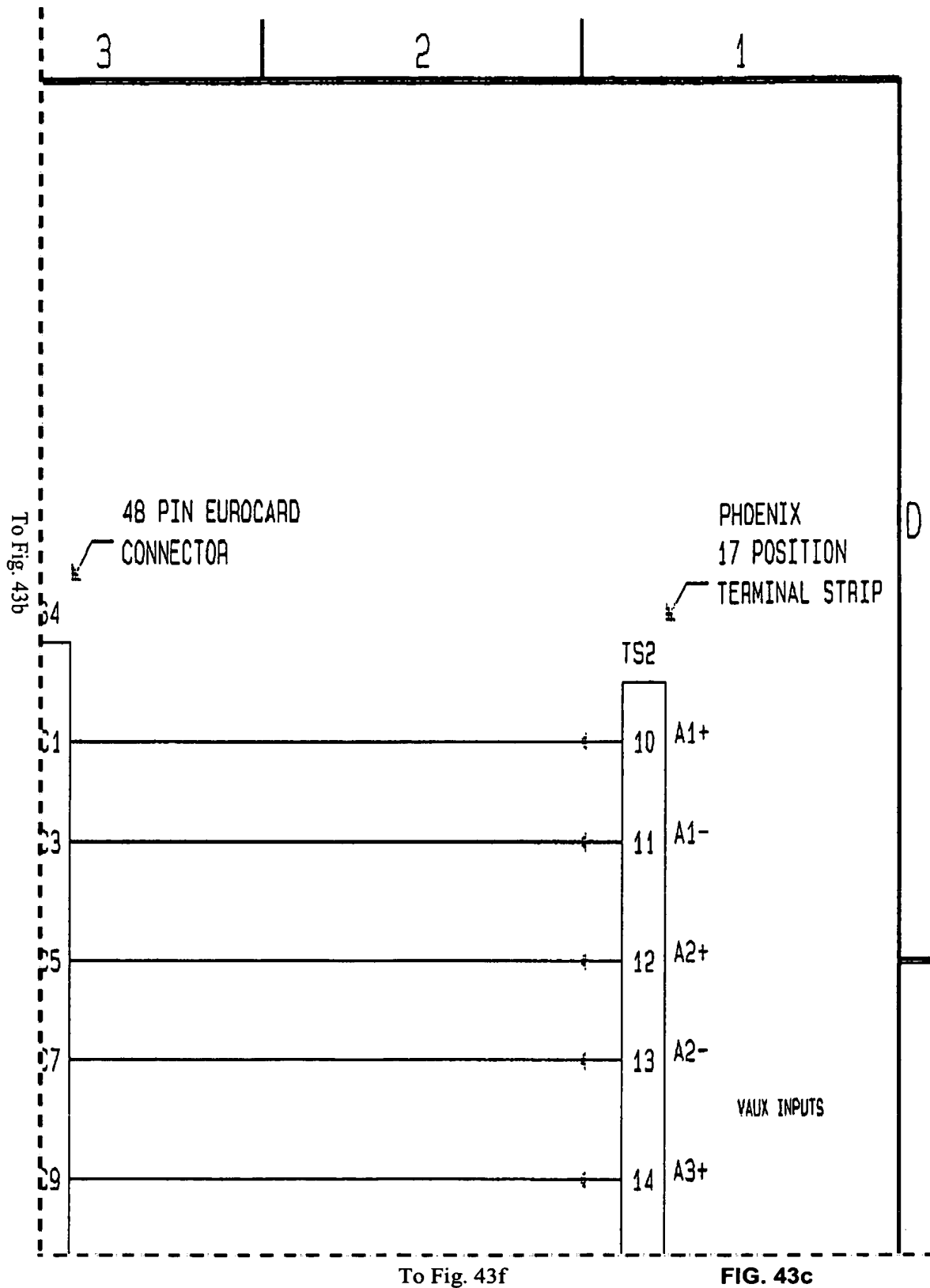
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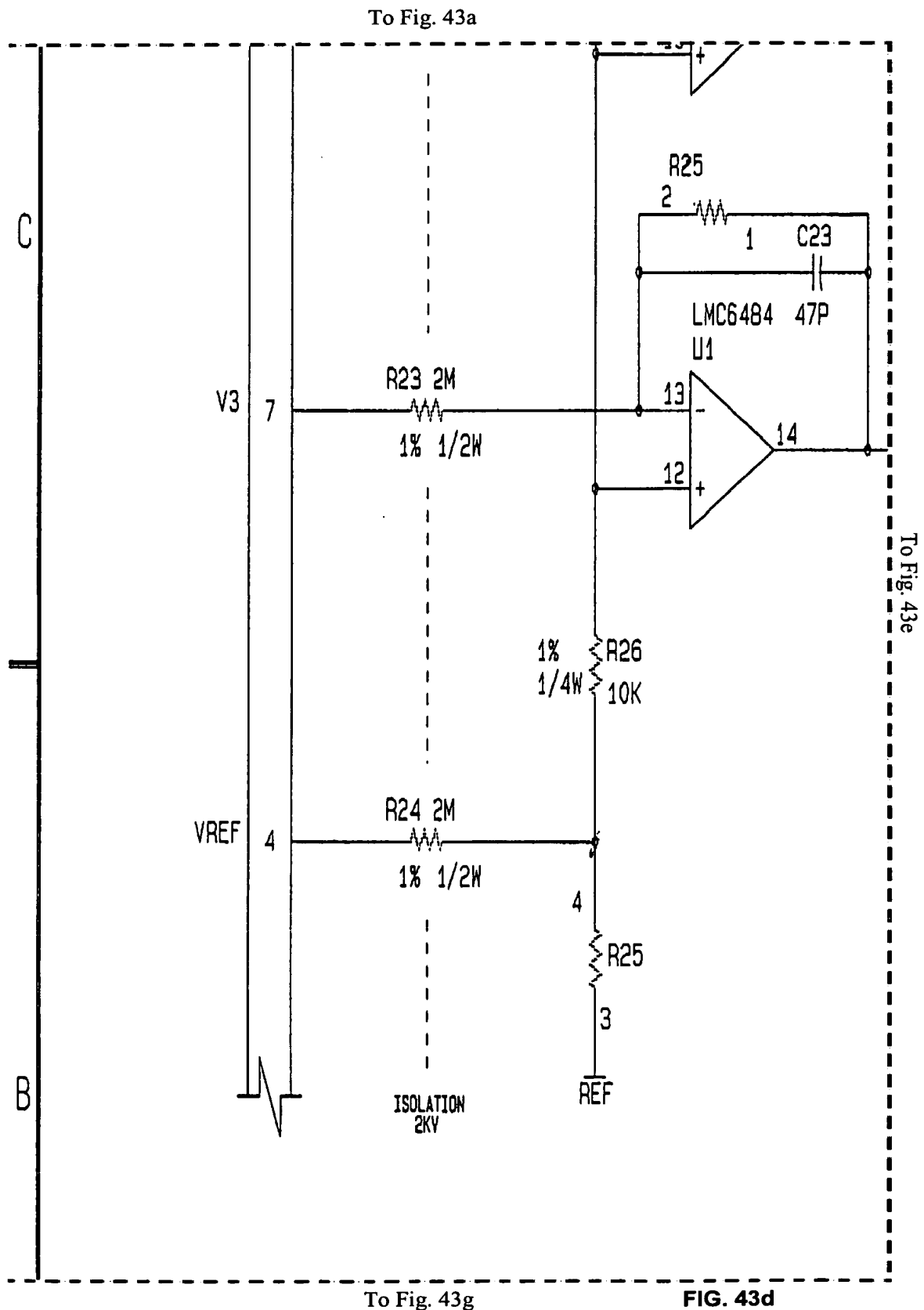
1

FIG. 42i

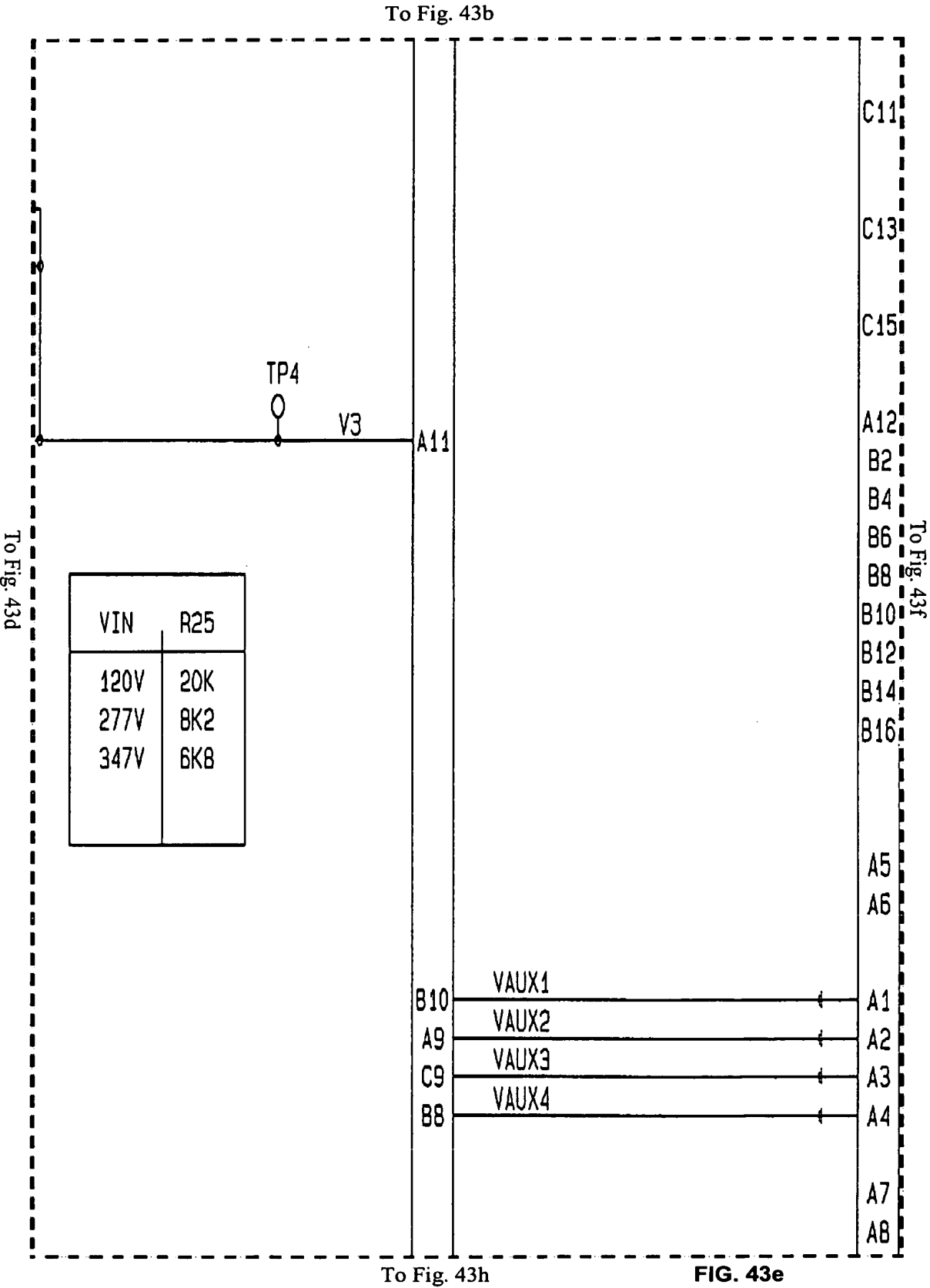












The diagram shows a multi-channel signal processing circuit. On the left, a vertical bus is labeled with pin numbers 1 through 18. Pins 11, 13, and 15 are connected to a horizontal bus on the right, which is labeled 15, 16, and 17 respectively. These are also labeled A3-, A4+, and A4-. A ground symbol is connected to the right bus at pin 15. Pins 12 through 16 are connected to a vertical bus on the right, which is labeled 12, 13, 14, 15, and 16 respectively. These are also labeled A1+, A2+, A3+, A4+, and A5+. A ground symbol is connected to the right bus at pin 12. Pins 17 and 18 are connected to a vertical bus on the right, which is labeled 17 and 18 respectively. These are also labeled A6+ and A7+. A ground symbol is connected to the right bus at pin 17. A +5V supply is connected to pin 7, and a +12V supply is connected to pin 8. A label 'To Fig. 43e' is present on the left side of the diagram.

FIG. 43f

To Fig. 43d

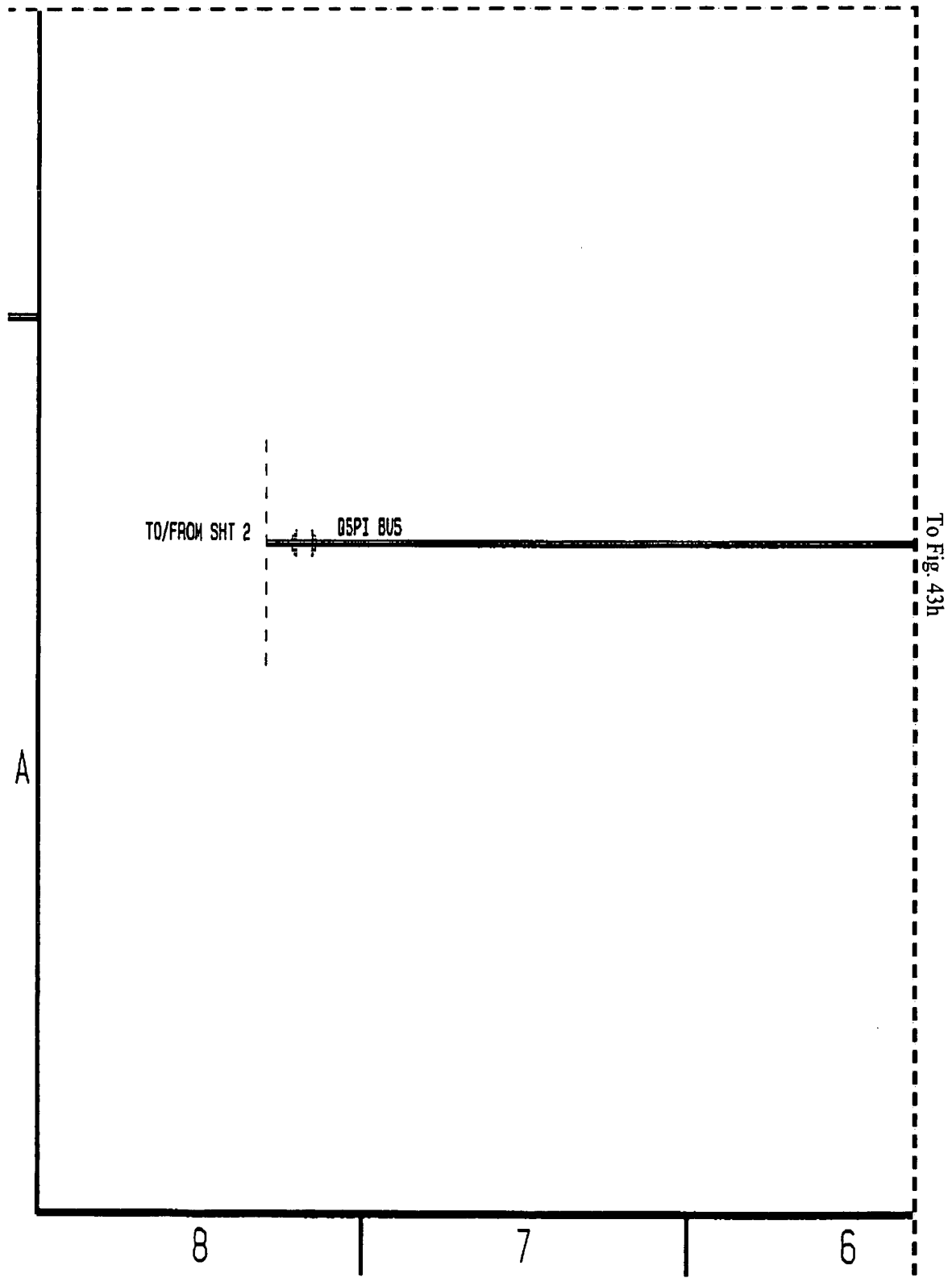
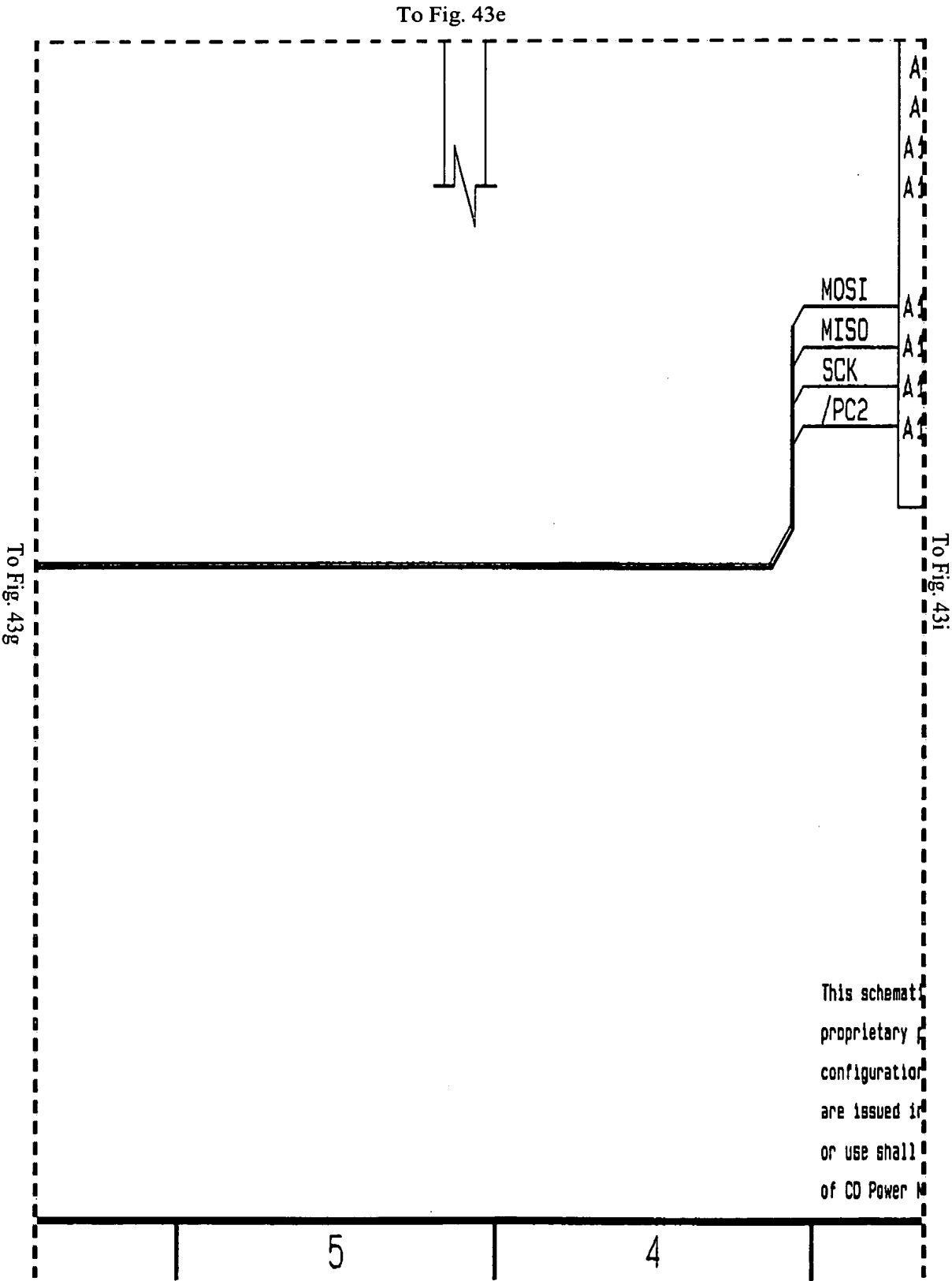


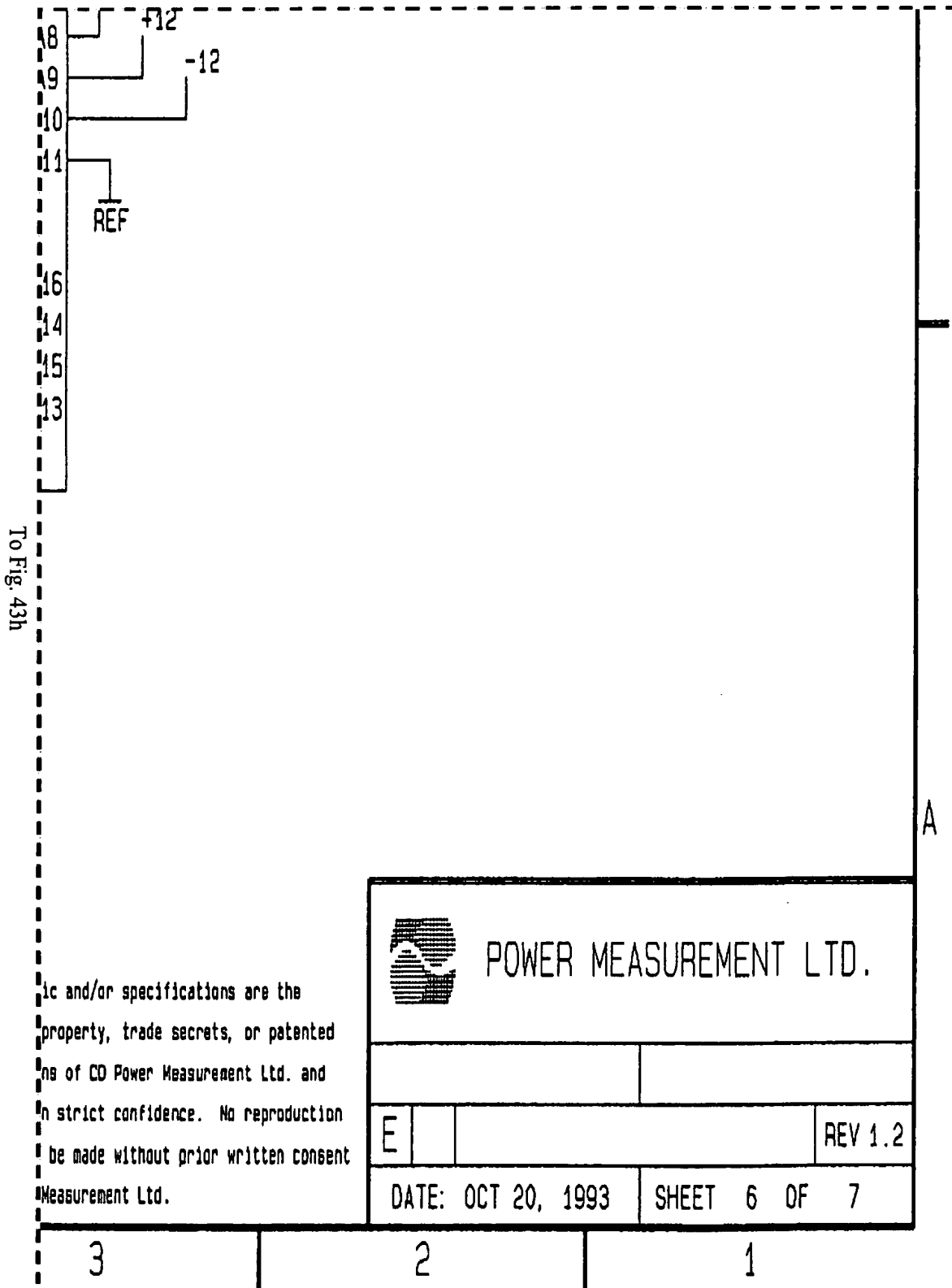
FIG. 43g



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FIG. 43h

To Fig. 43f



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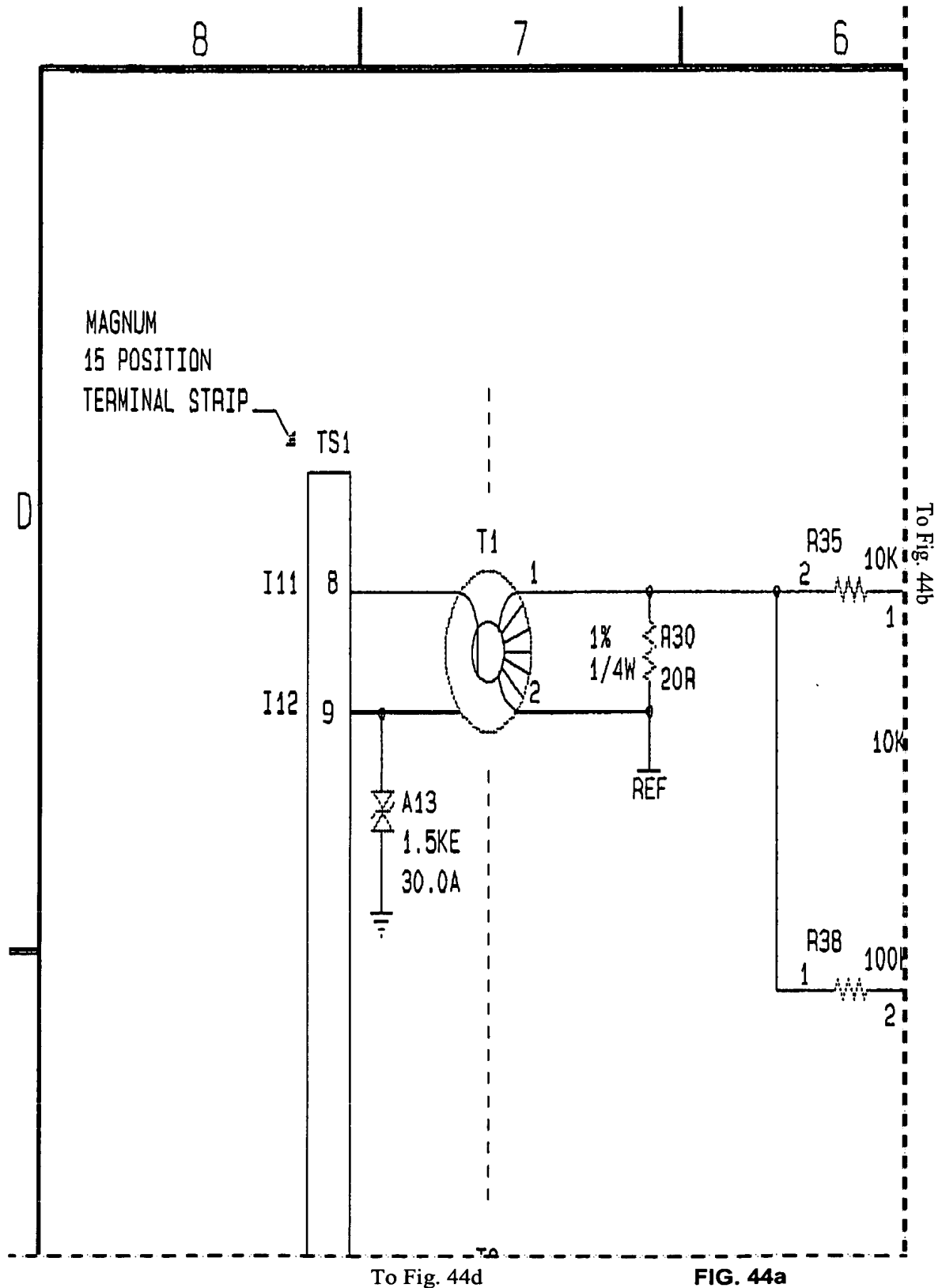
SHEET 6 OF 7

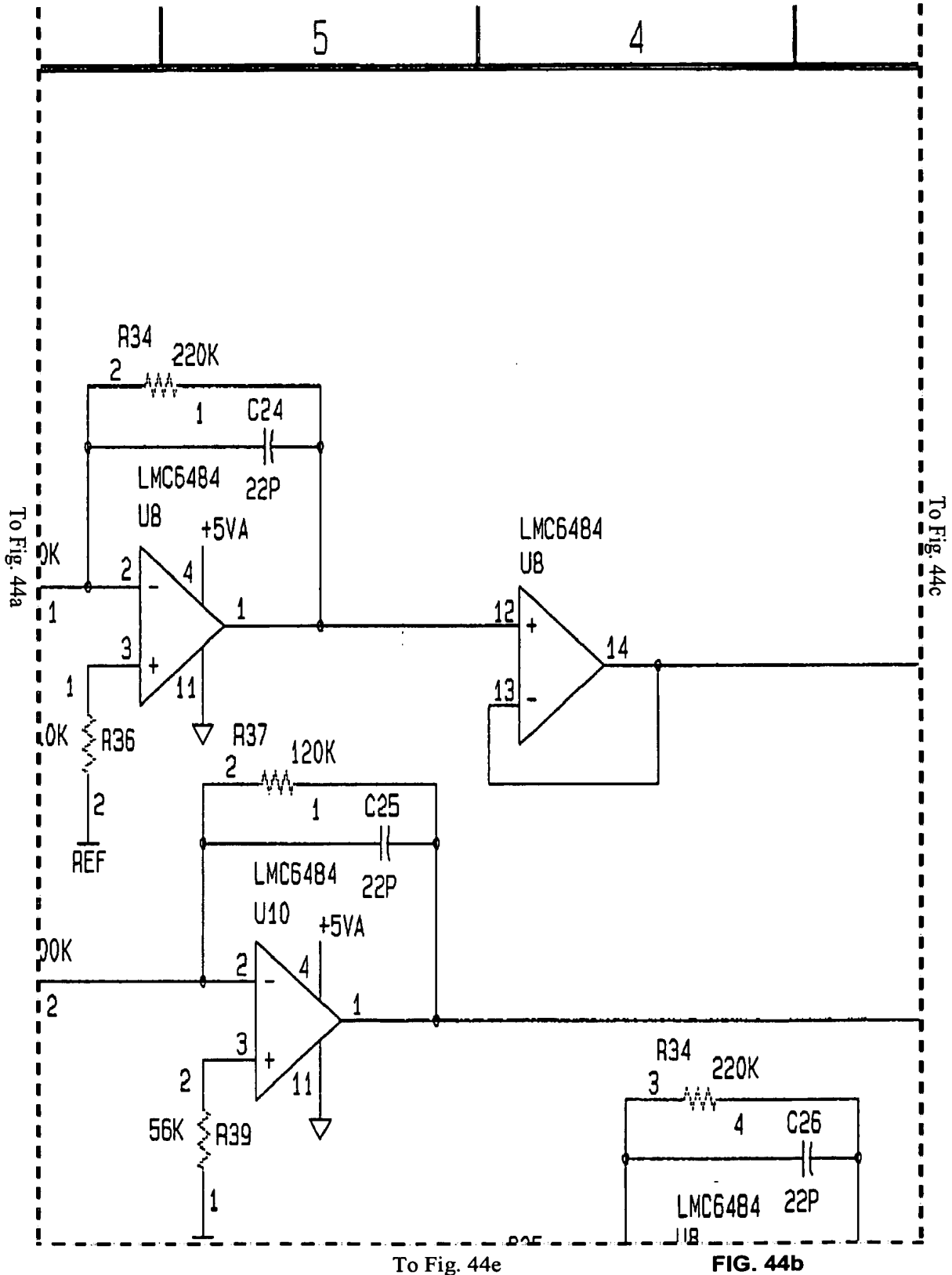
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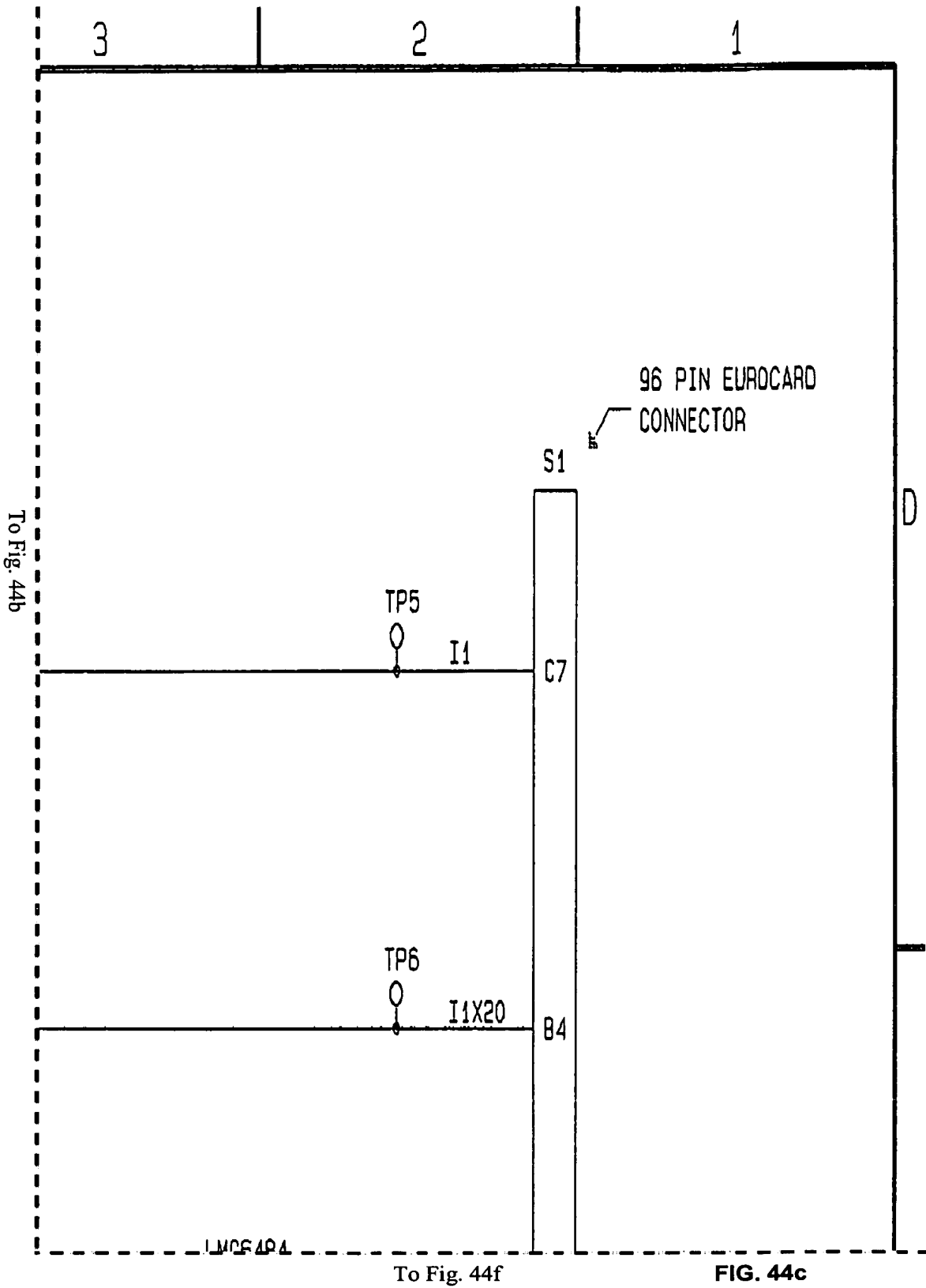
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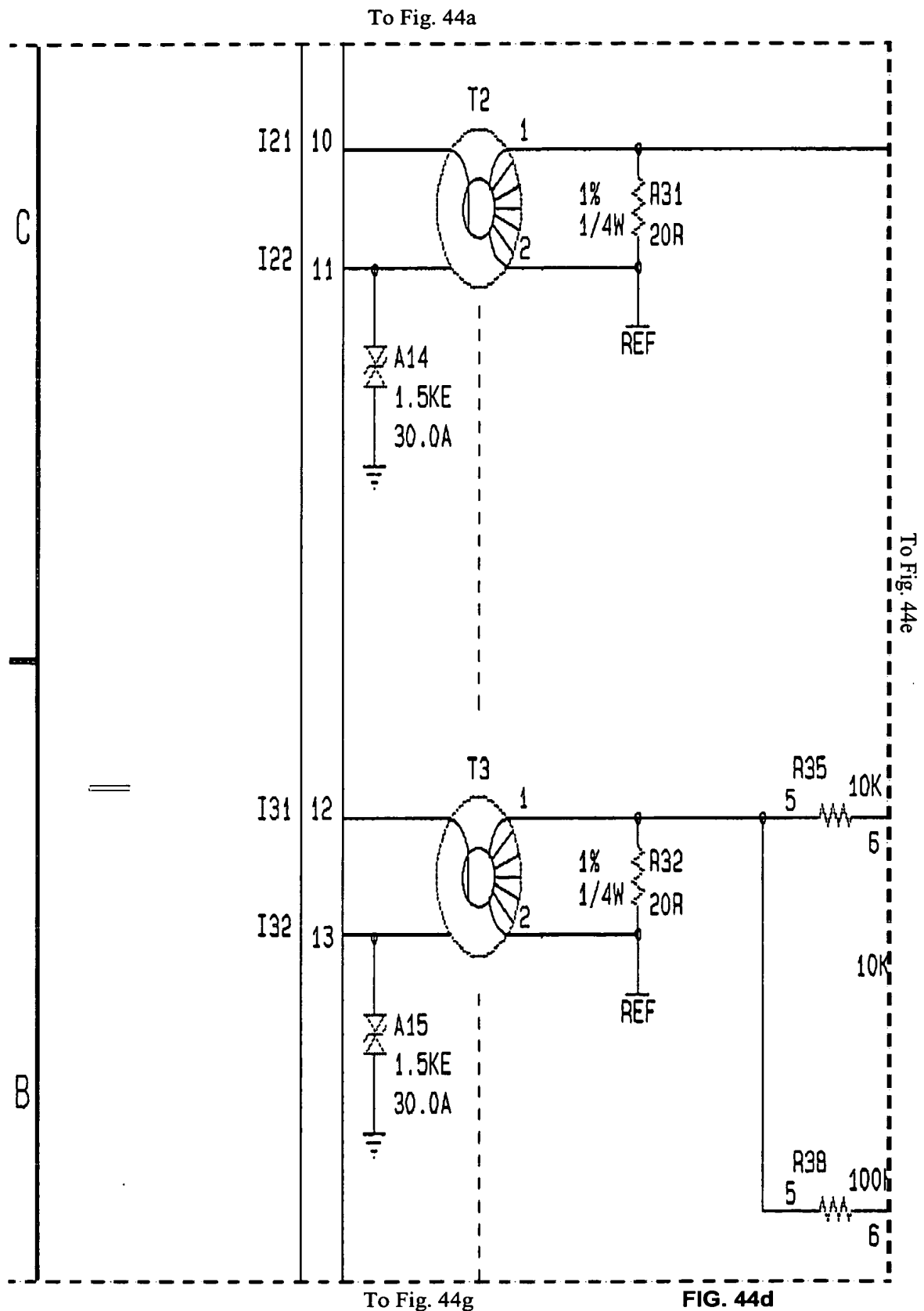
FIG. 43i



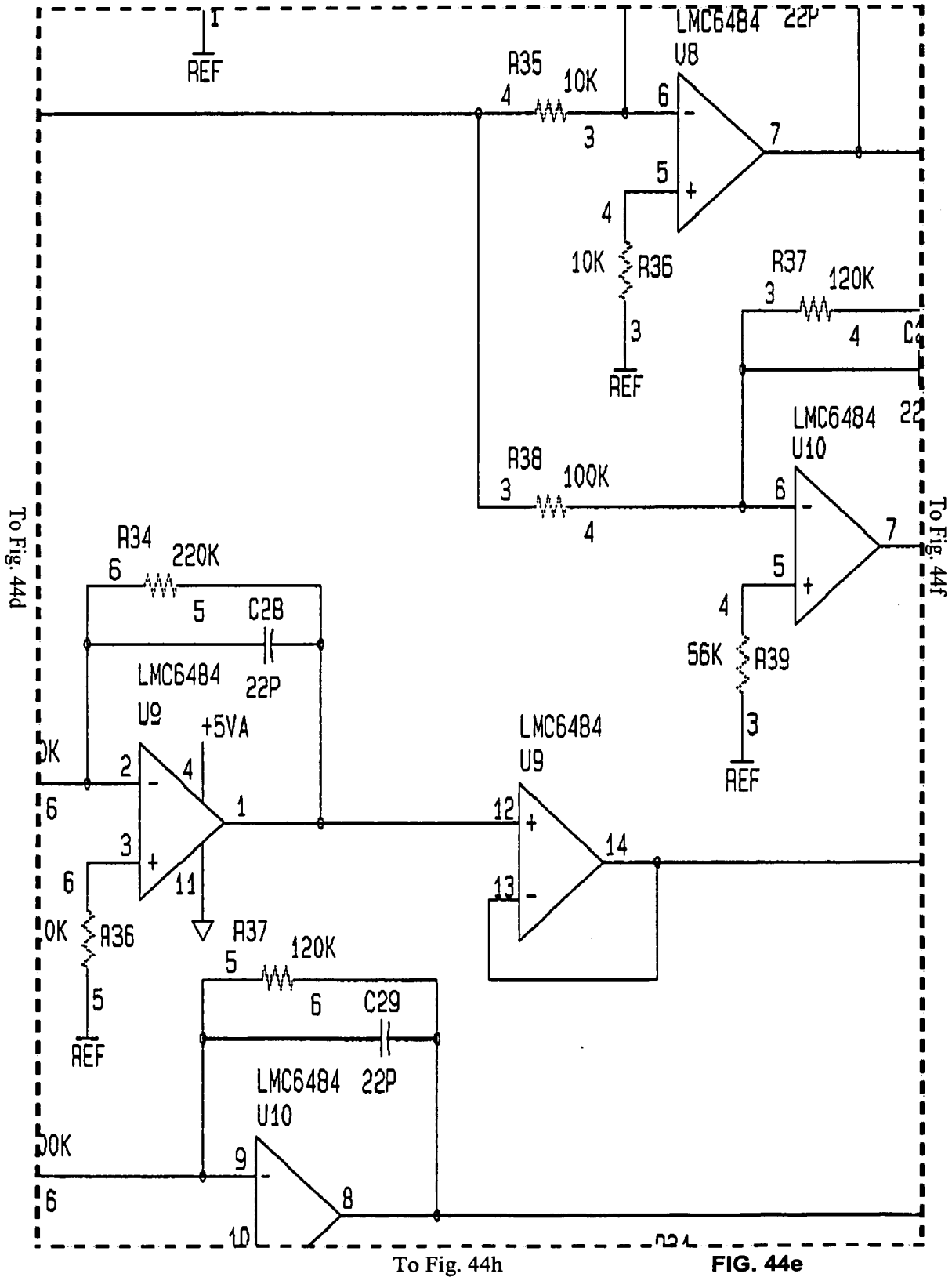








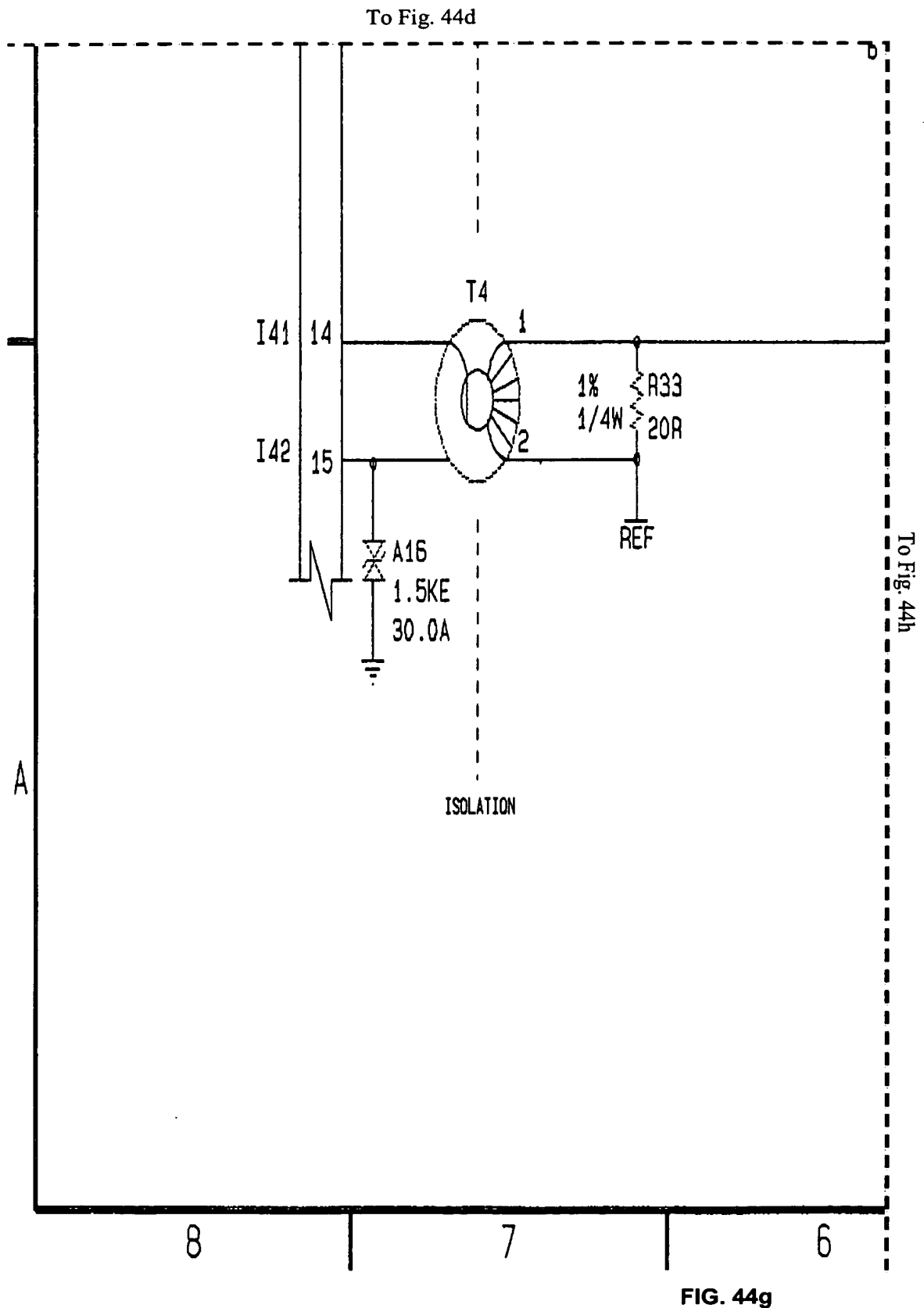
To Fig. 44b

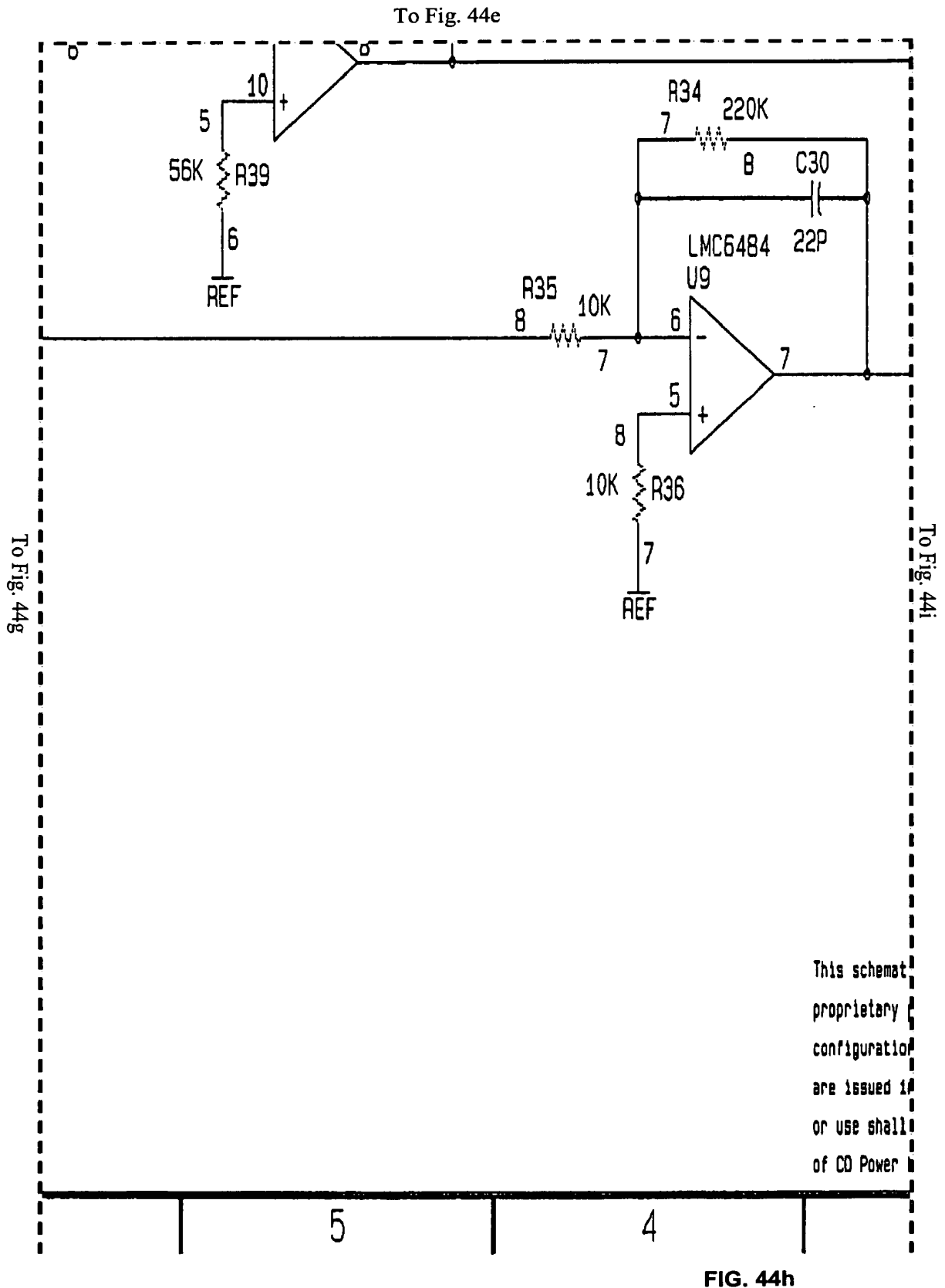


To Fig. 44h

FIG. 44e

**FIG. 44f**





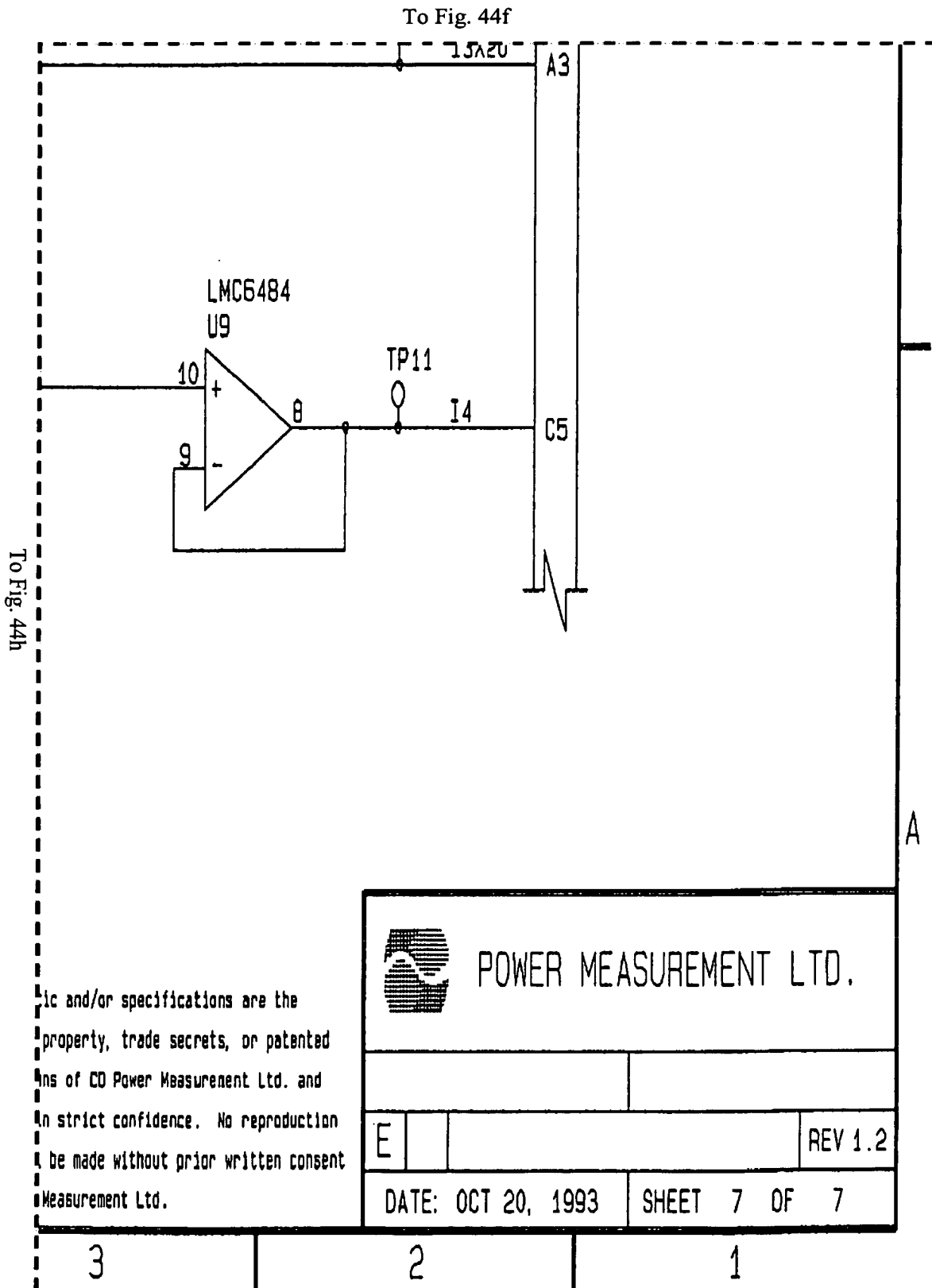
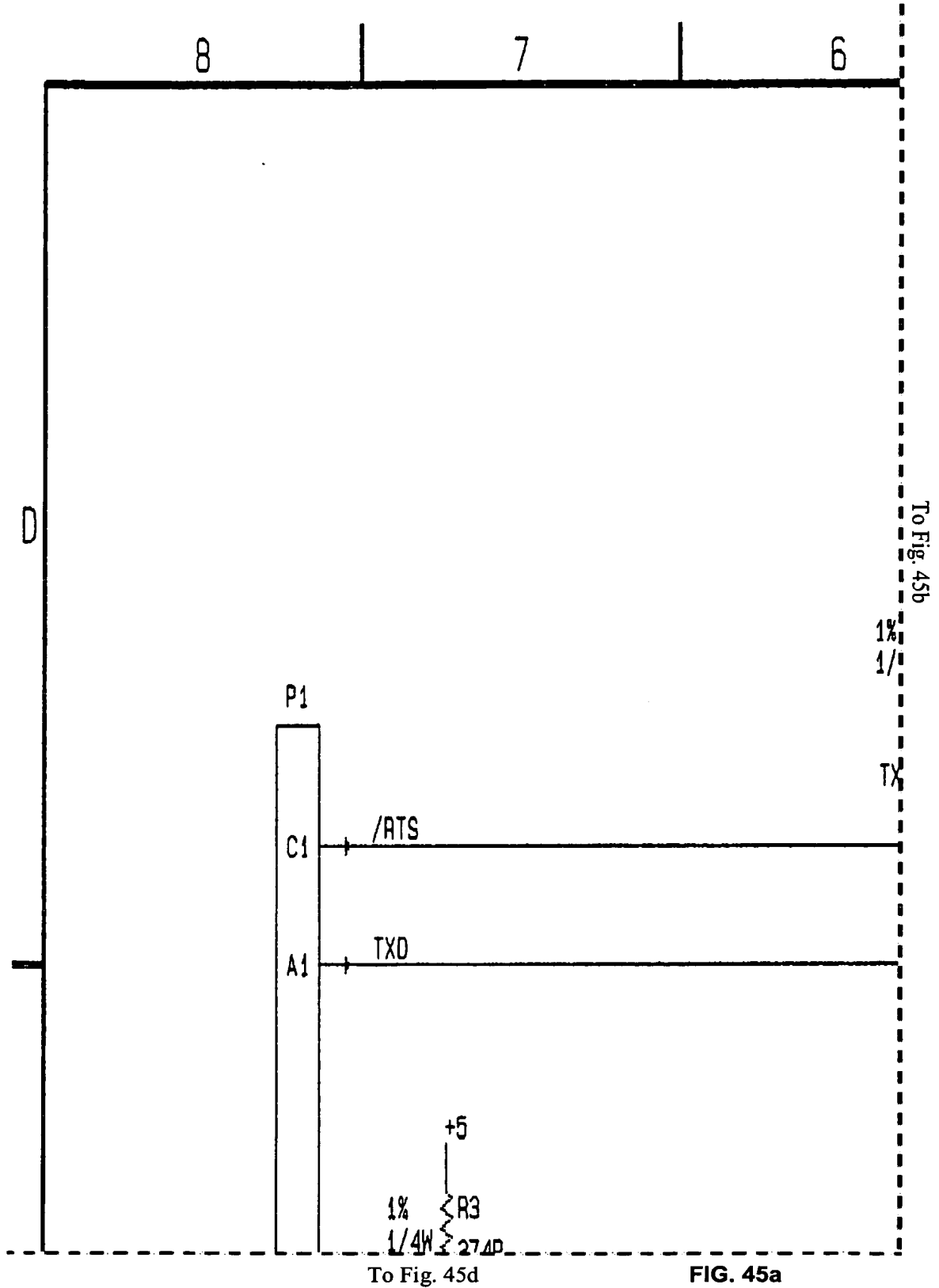
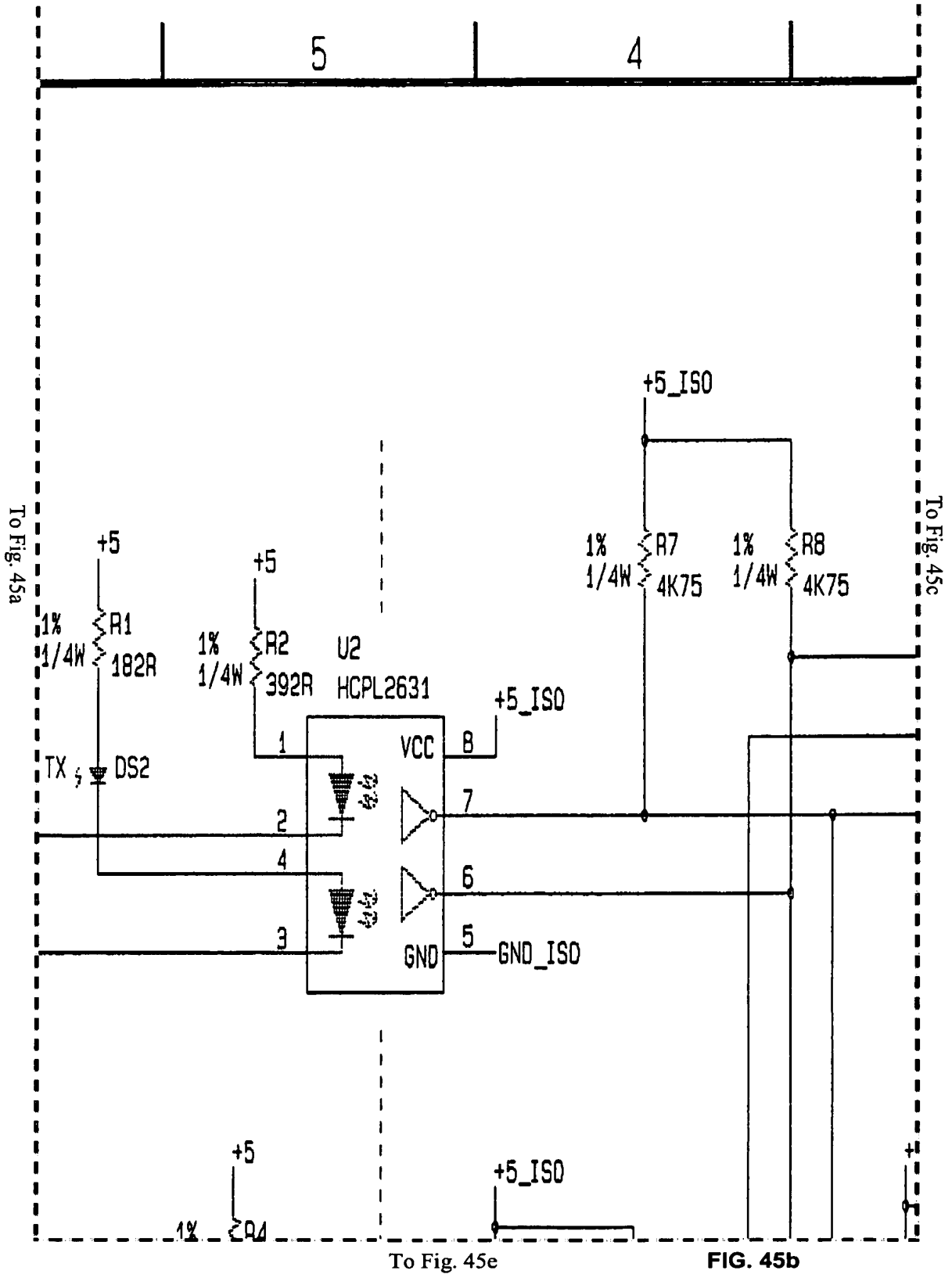
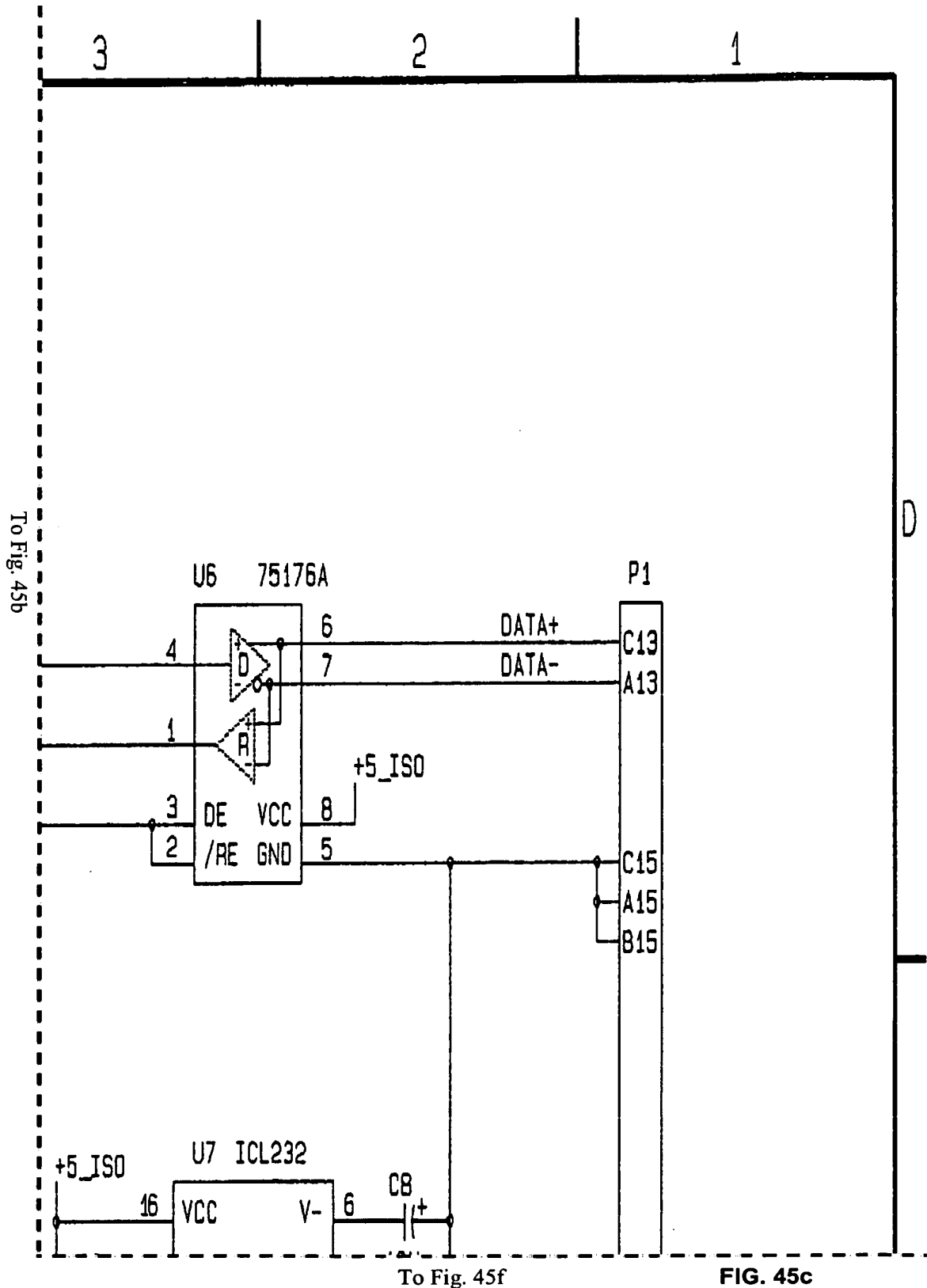


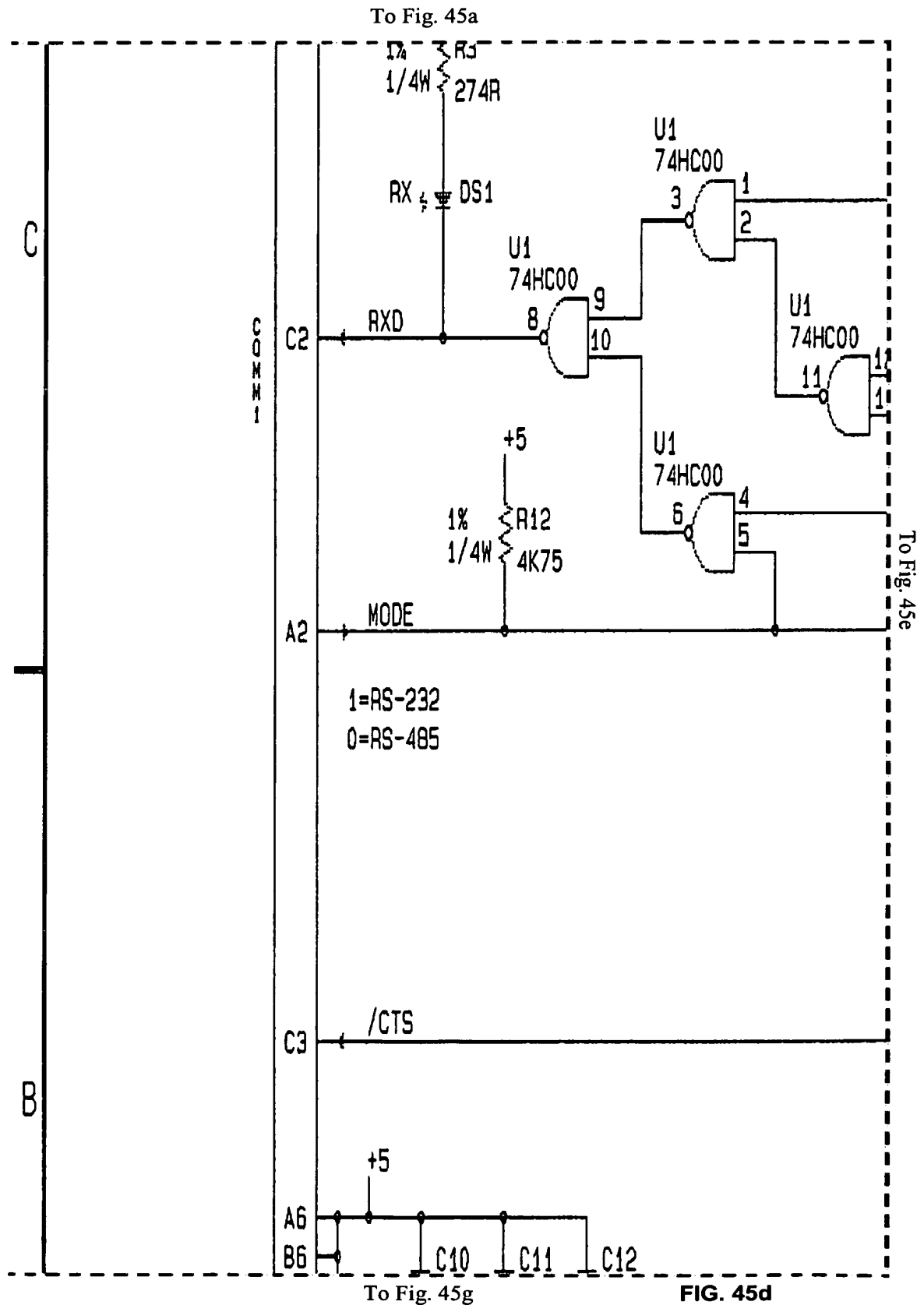
FIG. 44i



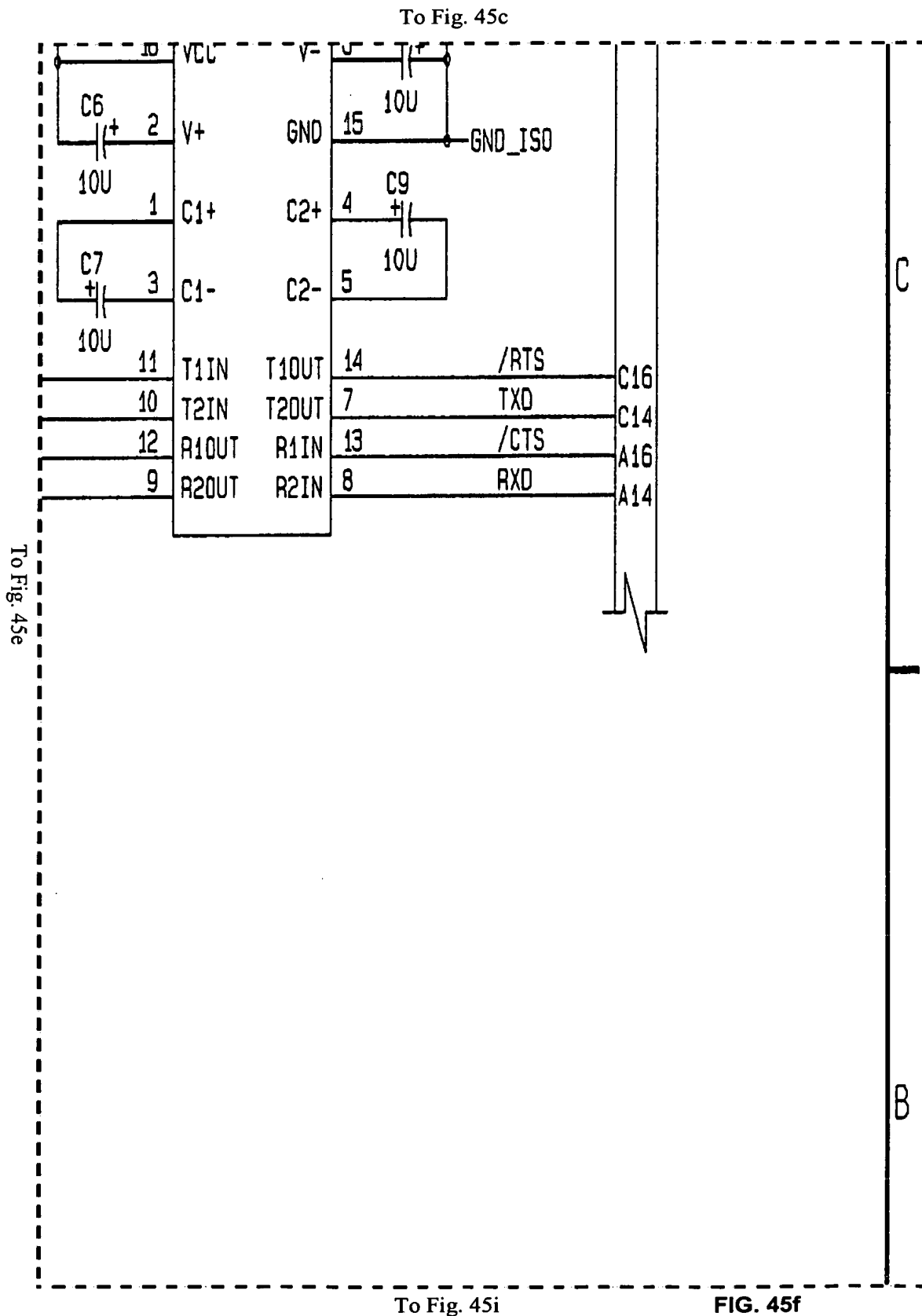




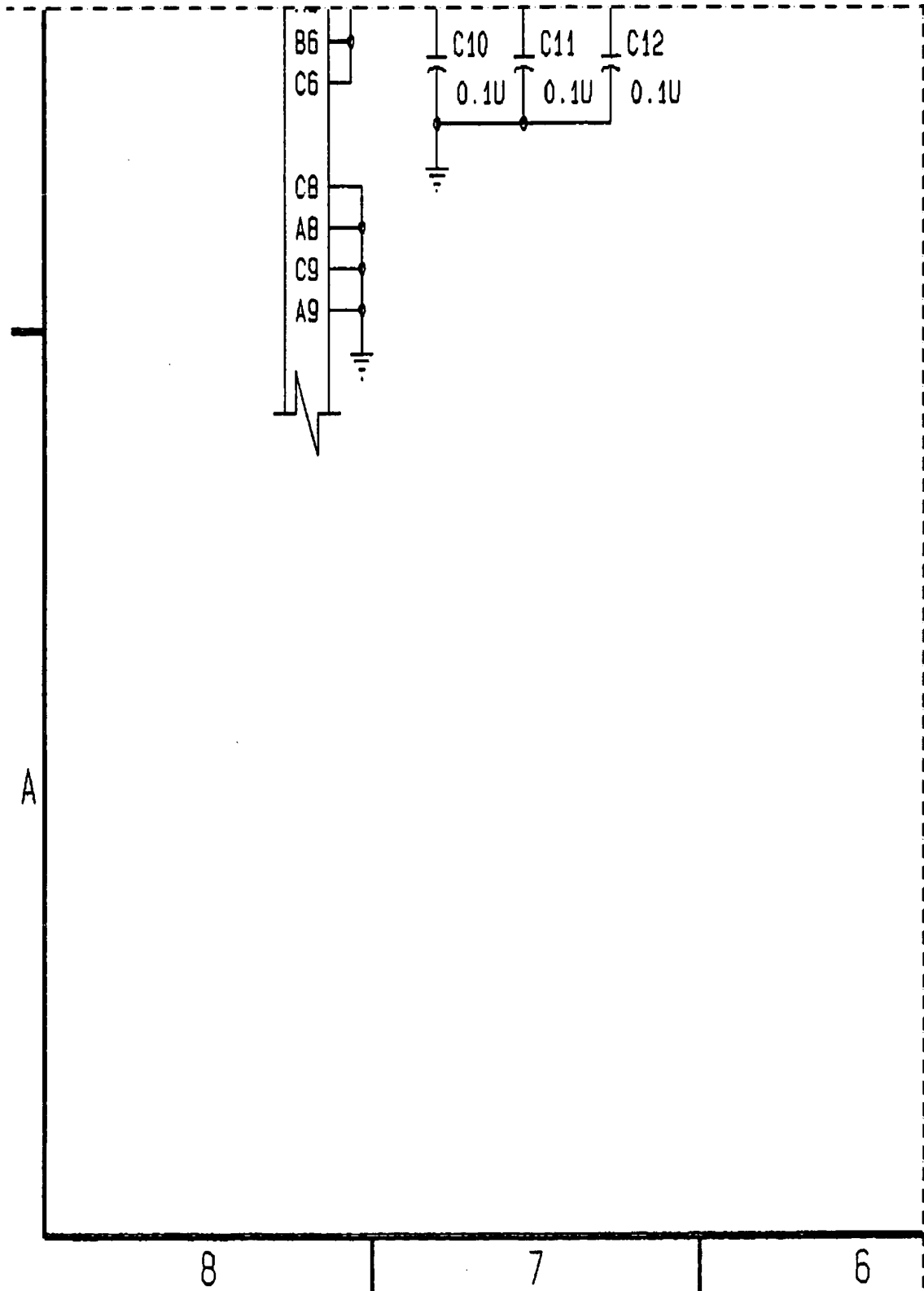








To Fig. 45d

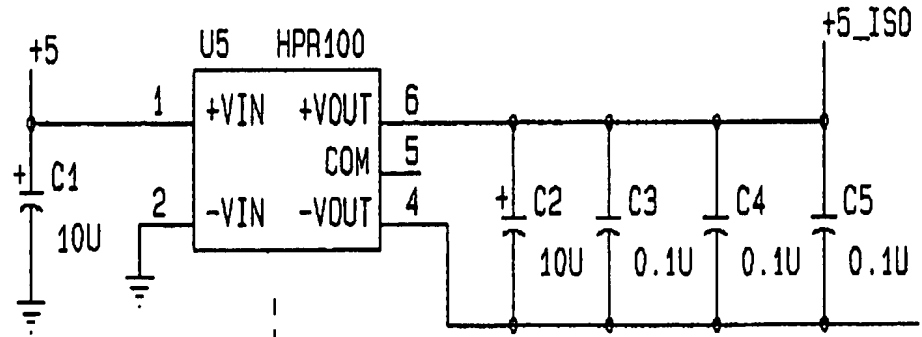


To Fig. 45h

FIG. 45g

To Fig. 45e

To Fig. 45g



To Fig. 45i

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5

4

FIG. 45h

To Fig. 45f

To Fig. 45h

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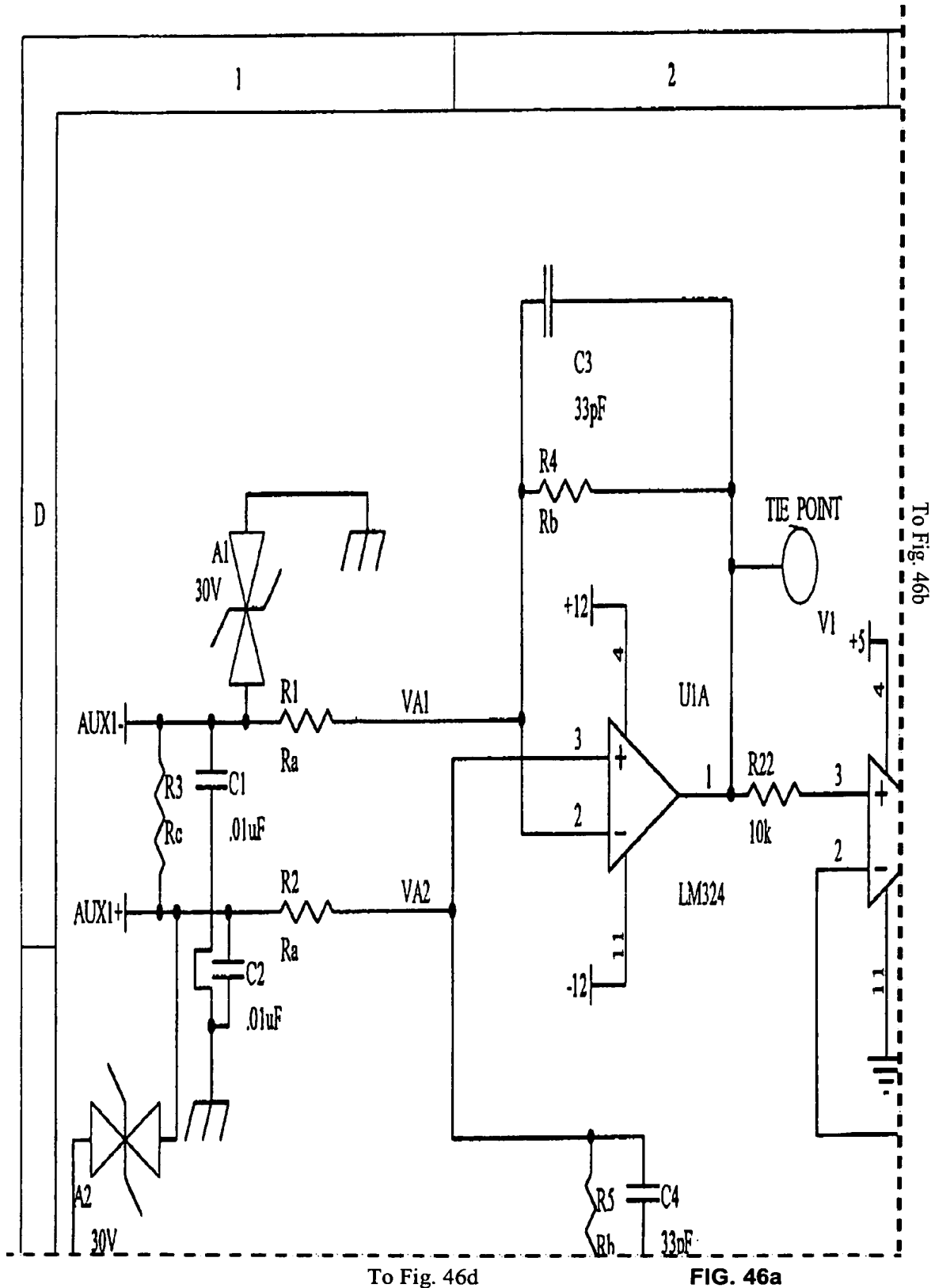
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DATE: JAN 7, 1993		SHEET 1 OF 1	

3

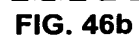
2

1

FIG. 45i







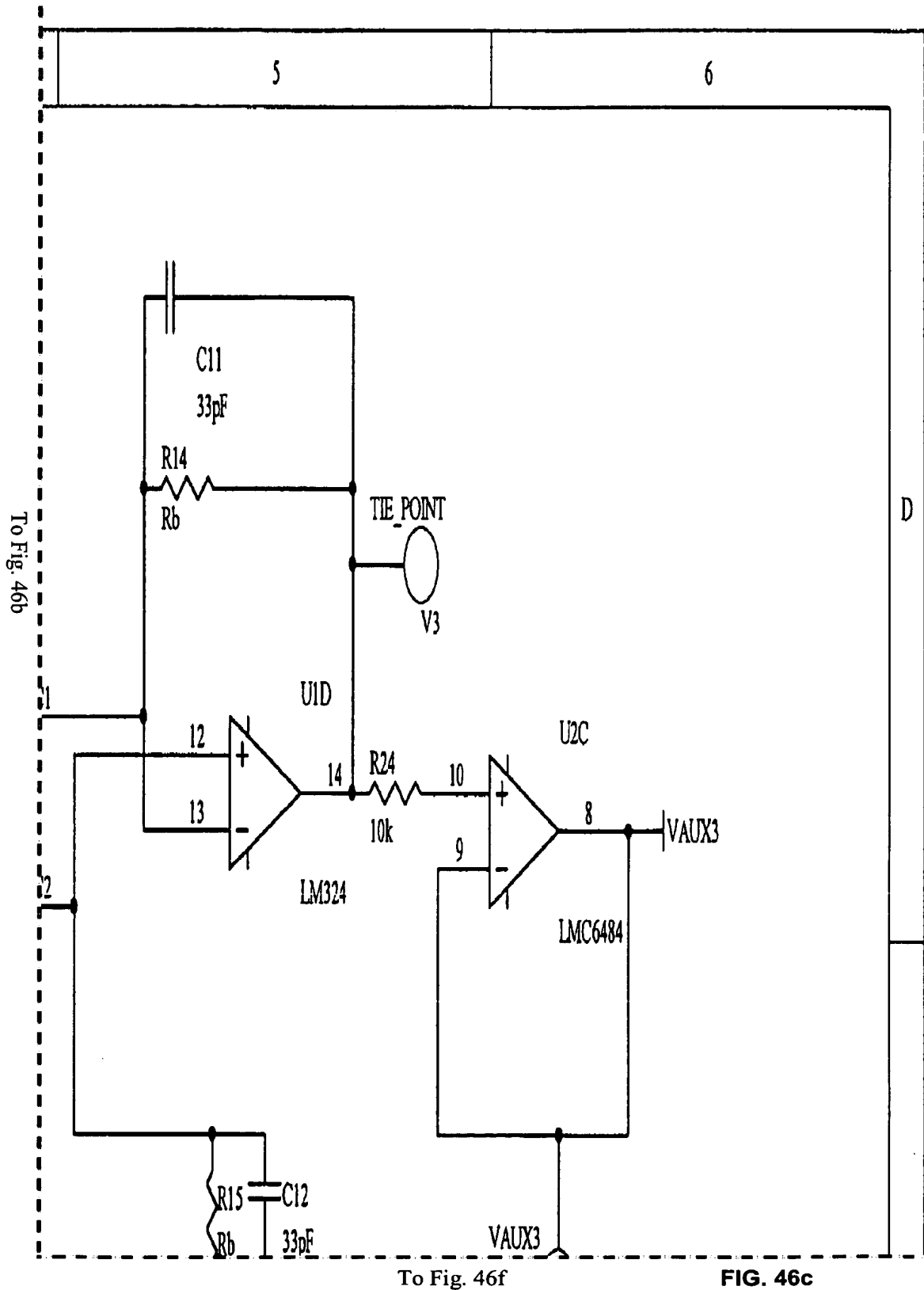
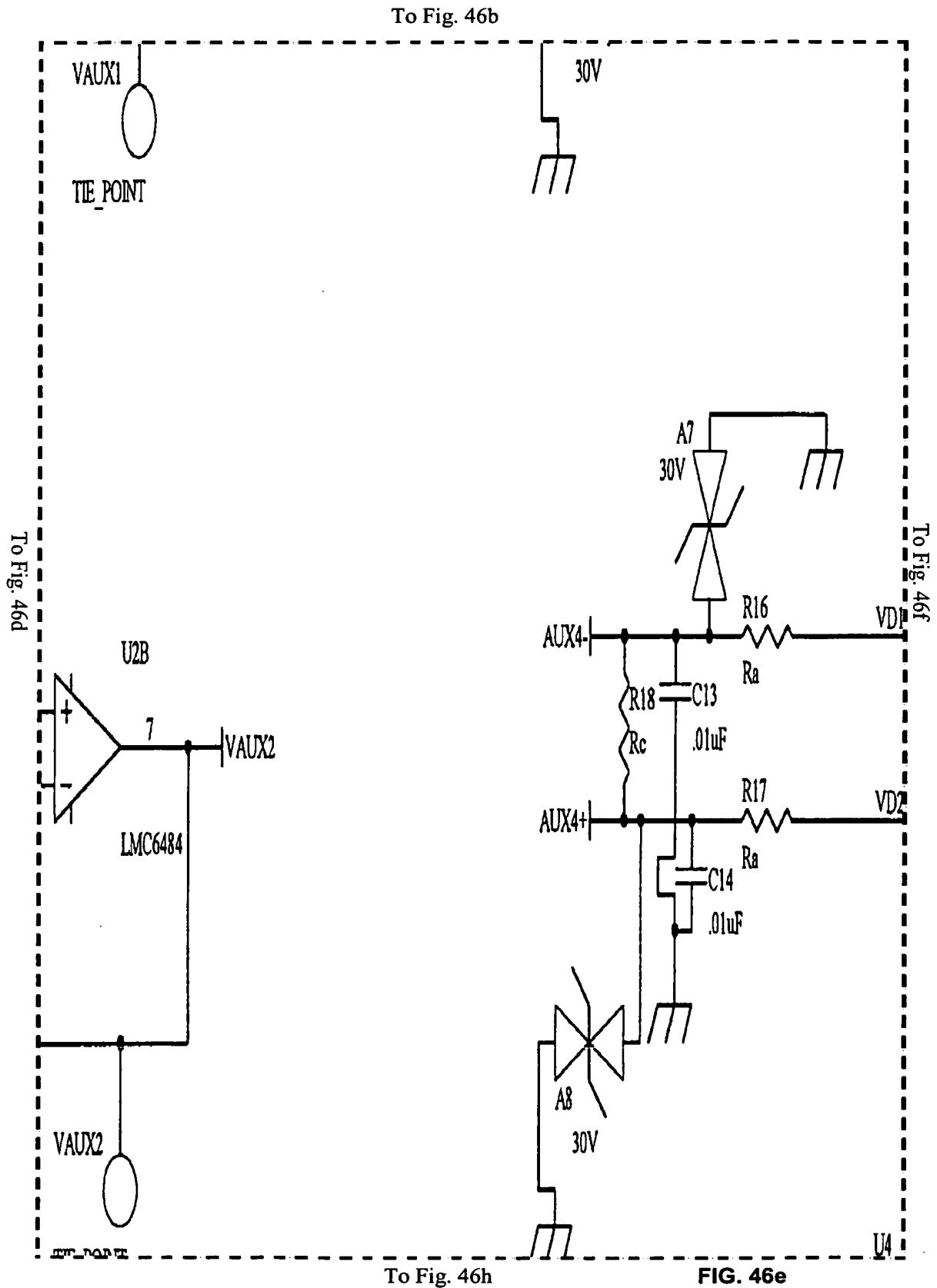
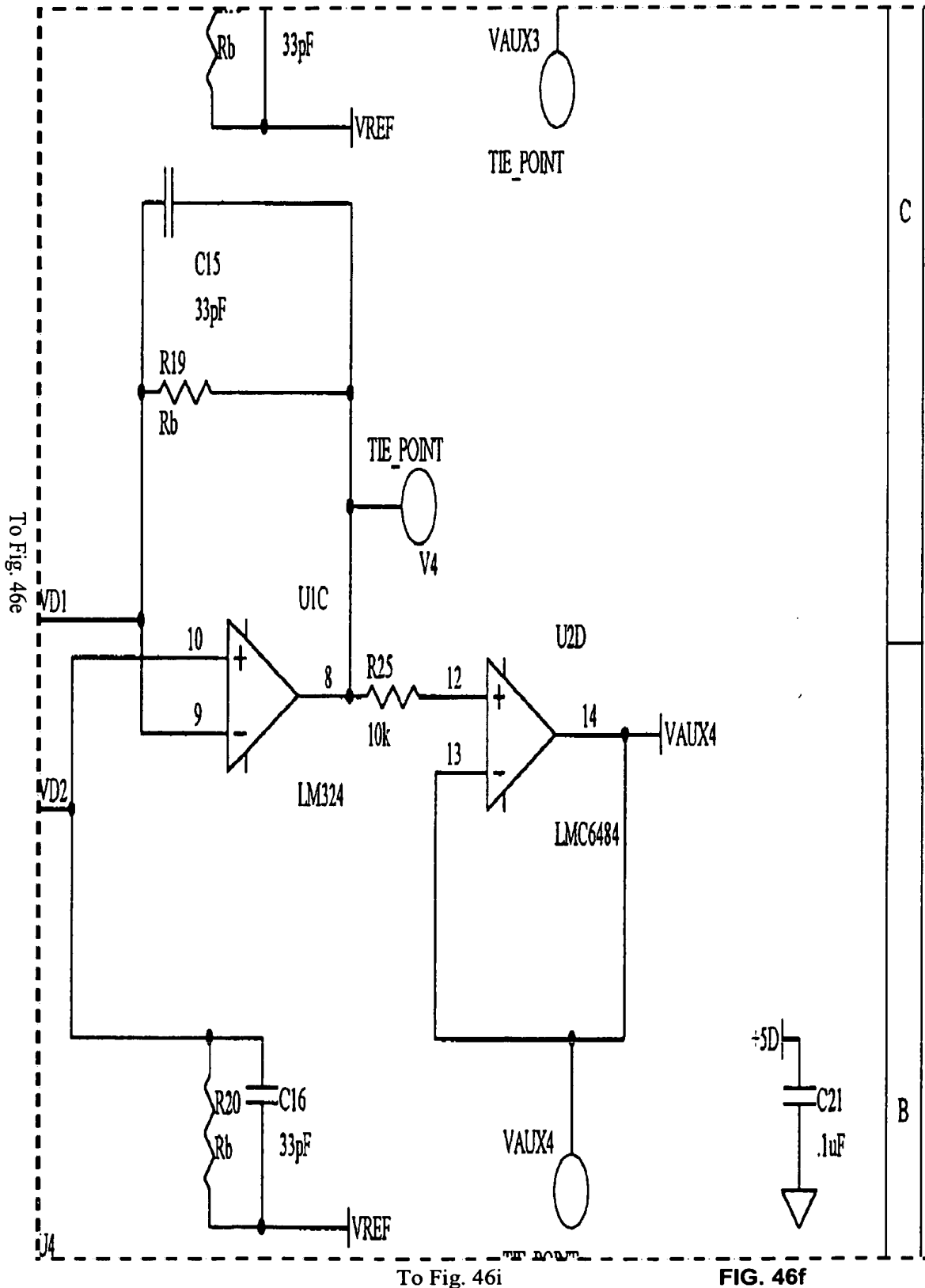


FIG. 46d



To Fig. 46c



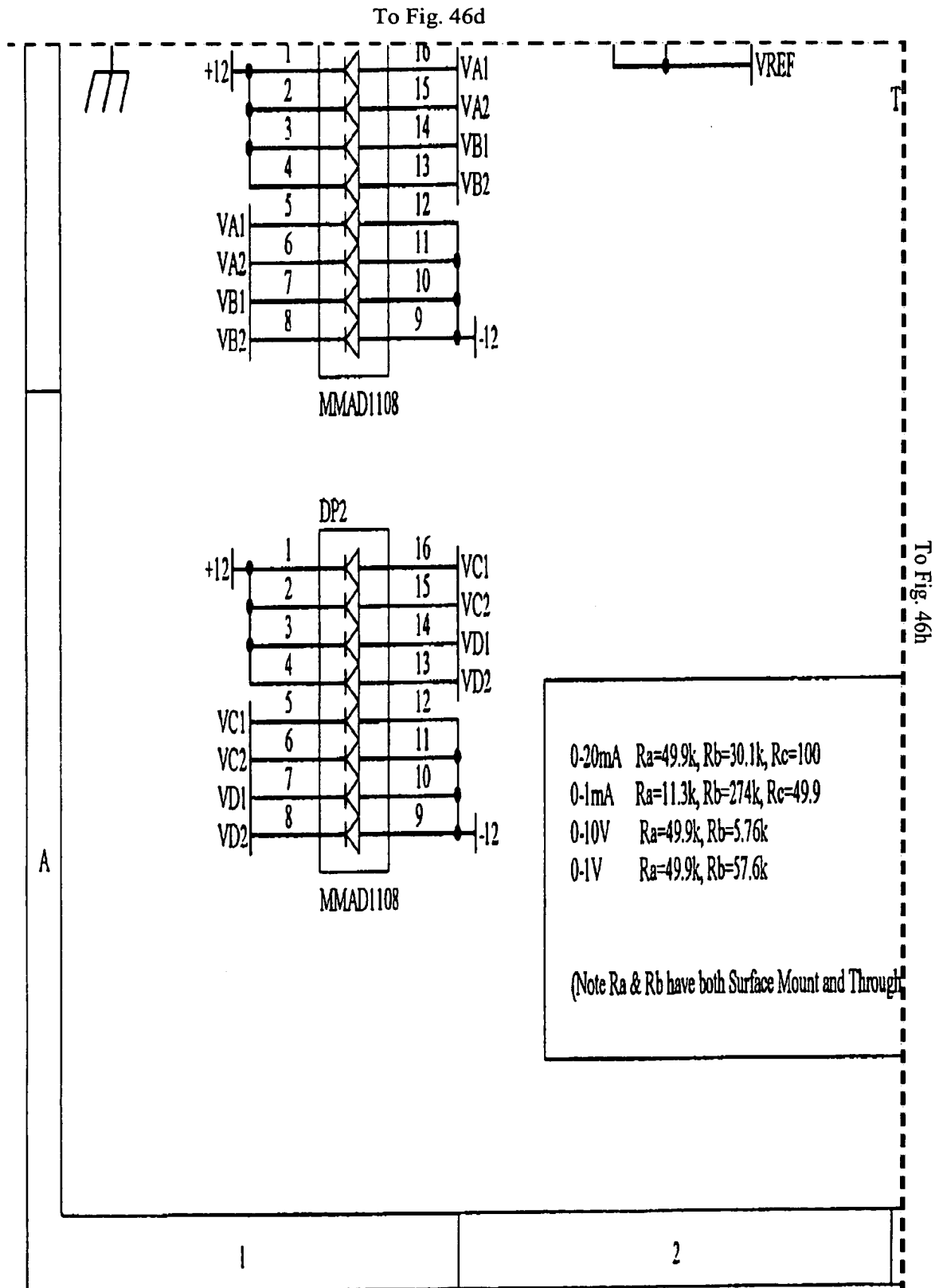


FIG. 46g

To Fig. 46e

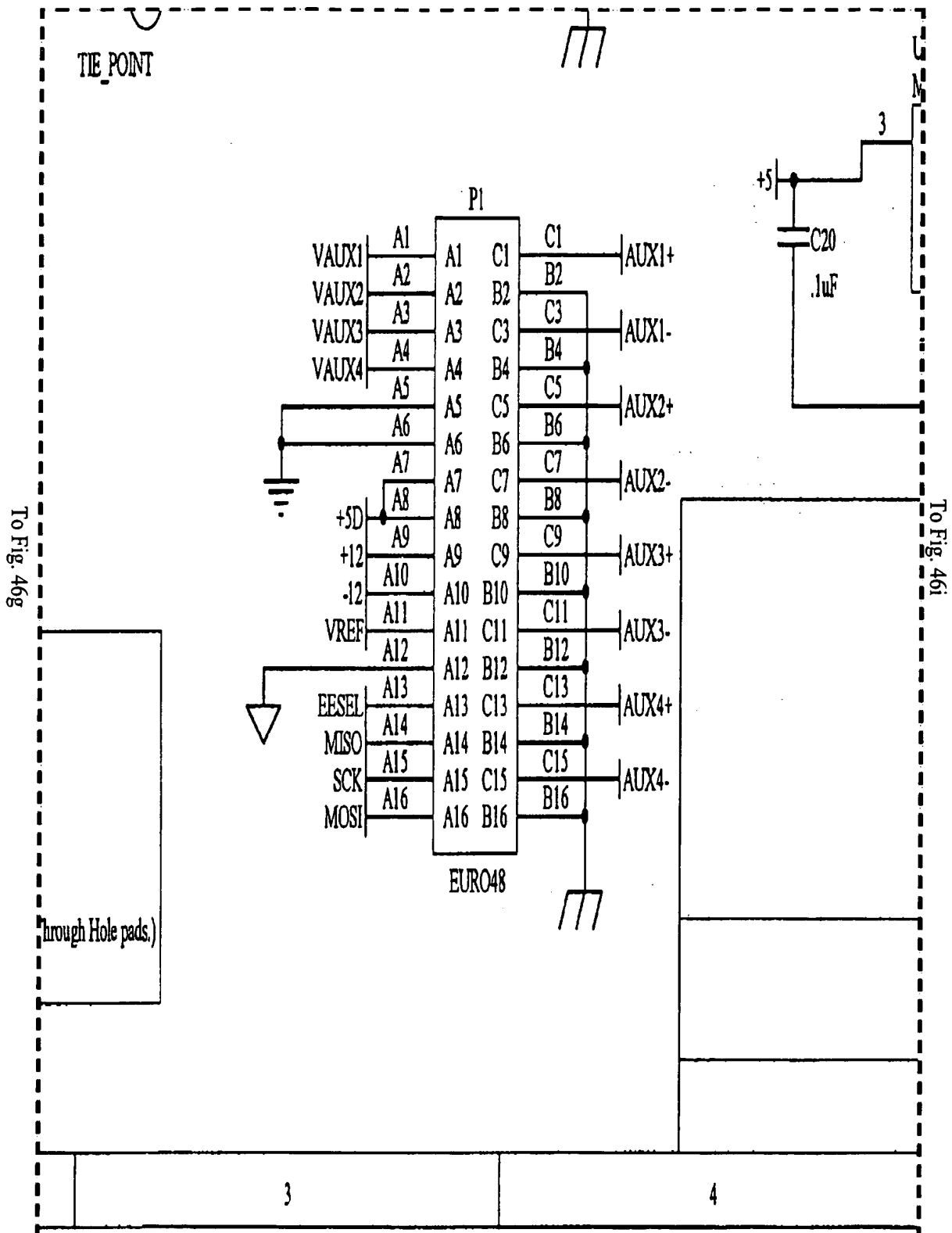
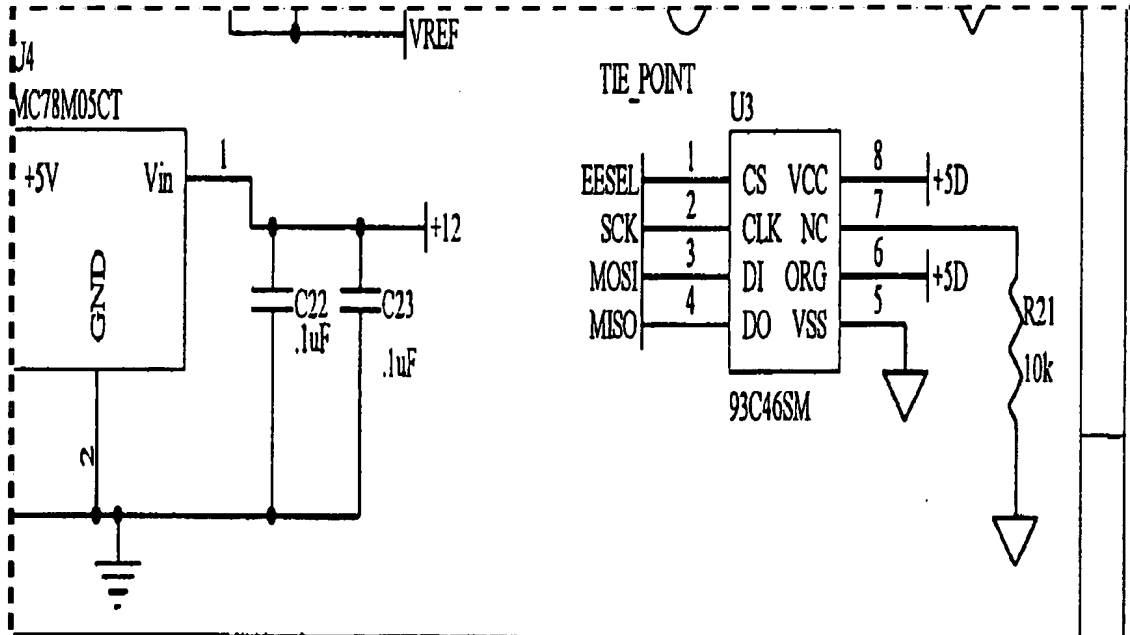


FIG. 46h

To Fig. 46f



To Fig. 46h

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Size	FCSM No.	DWG No.	Rev	
B		14000-0022	0.013	
Scale	Sheet		1 of 1	
5			6	

FIG. 46i